

Analysis and Validation Methodologies of Link Training and Speed Transition Test Cases

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Agenda

- Introduction
- Initial Training Analysis
- Transmitter and Receiver Equalization
- 8 Gig Speed Transition
- 16 Gig Speed Transition
- Violations Detected by PCI-SIG Compliance
- Violations Detected by Additional Validation Tests
- Automation of a Validation Test Suite
- Summary

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Introduction

- PCI Express® specifications are climbing up the speed ladder
- Speed transition Validation & analysis challenges increase
  - While 2.5 and 5 gig speeds use fixed de-emphasis, 8 and 16 gig speeds require Tx/Rx equalization.
  - 5 and 8 gig speeds are negotiated to the highest advertised speed, Transition to 16 Gig is stepping through an 8 Gig equalizer
- Analysis methods of link training and dynamic equalization
- Traffic generation techniques for speed transition validation
- Failure examples covered by PCI-SIG Compliance
  - Example: Phase transition time limits
- Not all incompliant behaviors covered by PCI-SIG Compliance
  - Example: Link training TS2 packets in Rec.RcvrCfg are less than 32 TS2 as required
- Incorporate a sequence of validation tests into a test automation environment.

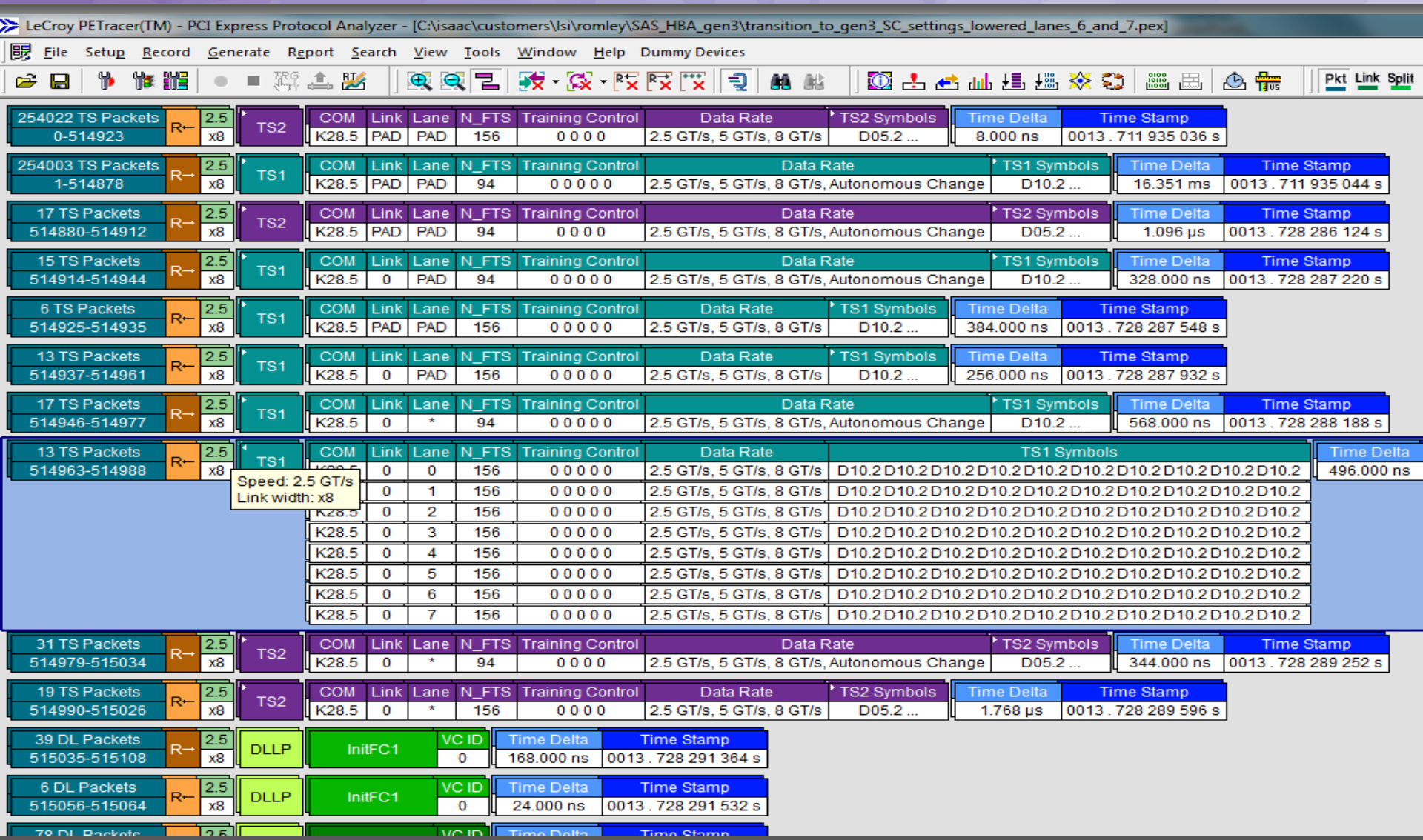
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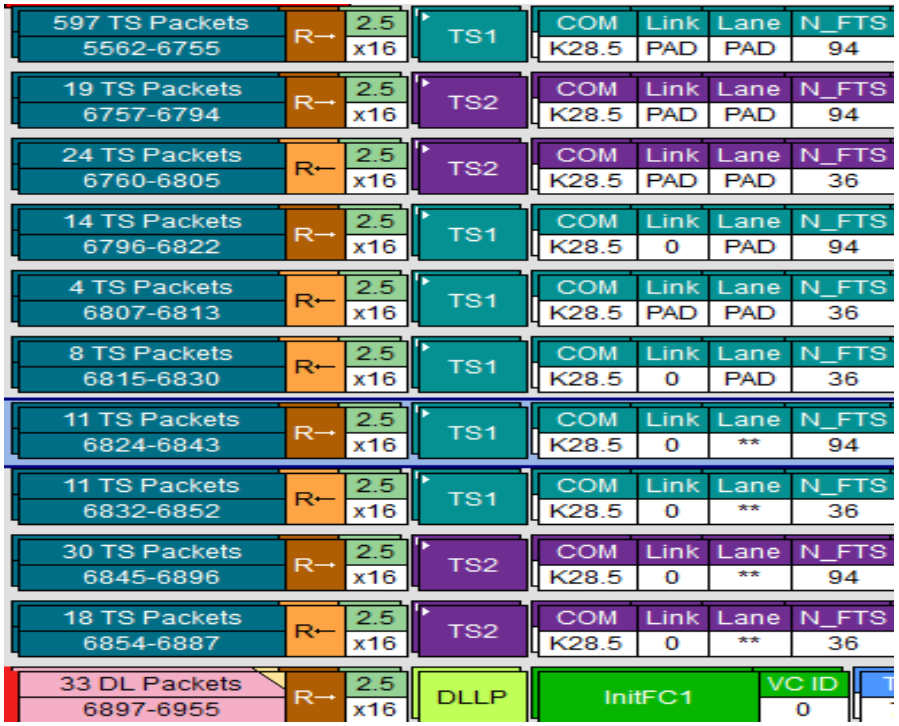
Initial Training



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Link/Lane Assignment Protocol

- Polling – TS1 / TS2 negotiation
- TS2 -> TS1 indicates transition to configuration
- Root assigns Link number
- EP follows
- Root assigns Lane numbers
- EP follows



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CTLE and DFE Equalization

- PCI Express 3.0 uses closed eye at device pins
- Eye opening performed through transmitter and receiver equalization
- Transmitter equalization uses 2 tap CTLE polynomial
- Receiver equalization uses CTLE and DFE equalizers
  - CTLE – Continuous Time Linear Equalizer, open loop transfer function
  - DFE – Differential feedback equalizer, feedback transfer function
  - DFE needed to encounter ISI
- Transfer function description
  - Pre-cursor – pre-shoot or boost
  - Post cursor – de-emphasis
- CTLE polynomial can be described using preset space or coefficient space
  - Preset space used for course equalization
  - Coefficient space used for fine tuning in increments of 1/24
  - PCI-SIG predefined presets used in terms of actual pre-cursor, cursor and post cursor gain

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CTLE Presets

- CTLE can be described by either presets or coefficients
- Presets use direct pre-shoot, boost and de-emphasis levels
- Course equalization through 10 pre-defined presets

Preset space

Table 4-16: Tx Preset Ratios and Corresponding Coefficient Values

Preset Number	Preshoot (dB)	De-emphasis (dB)	c_{-1}	c_{+1}	Va/Vd	Vb/Vd	Vc/Vd
P4	0.0	0.0	0.000	0.000	1.000	1.000	1.000
P1	0.0	-3.5 ± 1 dB	0.000	-0.167	1.000	0.668	0.668
P0	0.0	-6.0 ± 1.5 dB	0.000	-0.250	1.000	0.500	0.500
P9	3.5 ± 1 dB	0.0	-0.166	0.000	0.668	0.668	1.000
P8	3.5 ± 1 dB	-3.5 ± 1 dB	-0.125	-0.125	0.750	0.500	0.750
P7	3.5 ± 1 dB	-6.0 ± 1.5 dB	-0.100	-0.200	0.800	0.400	0.600
P5	1.9 ± 1 dB	0.0	-0.100	0.000	0.800	0.800	1.000
P6	2.5 ± 1 dB	0.0	-0.125	0.000	0.750	0.750	1.000
P3	0.0	-2.5 ± 1 dB	0.000	-0.125	1.000	0.750	0.750
P2	0.0	-4.4 ± 1.5 dB	0.000	-0.200	1.000	0.600	0.600
P10	0.0	See Note 2.	0.000	See Note 2.	1.000	See Note 2.	See Note 2.

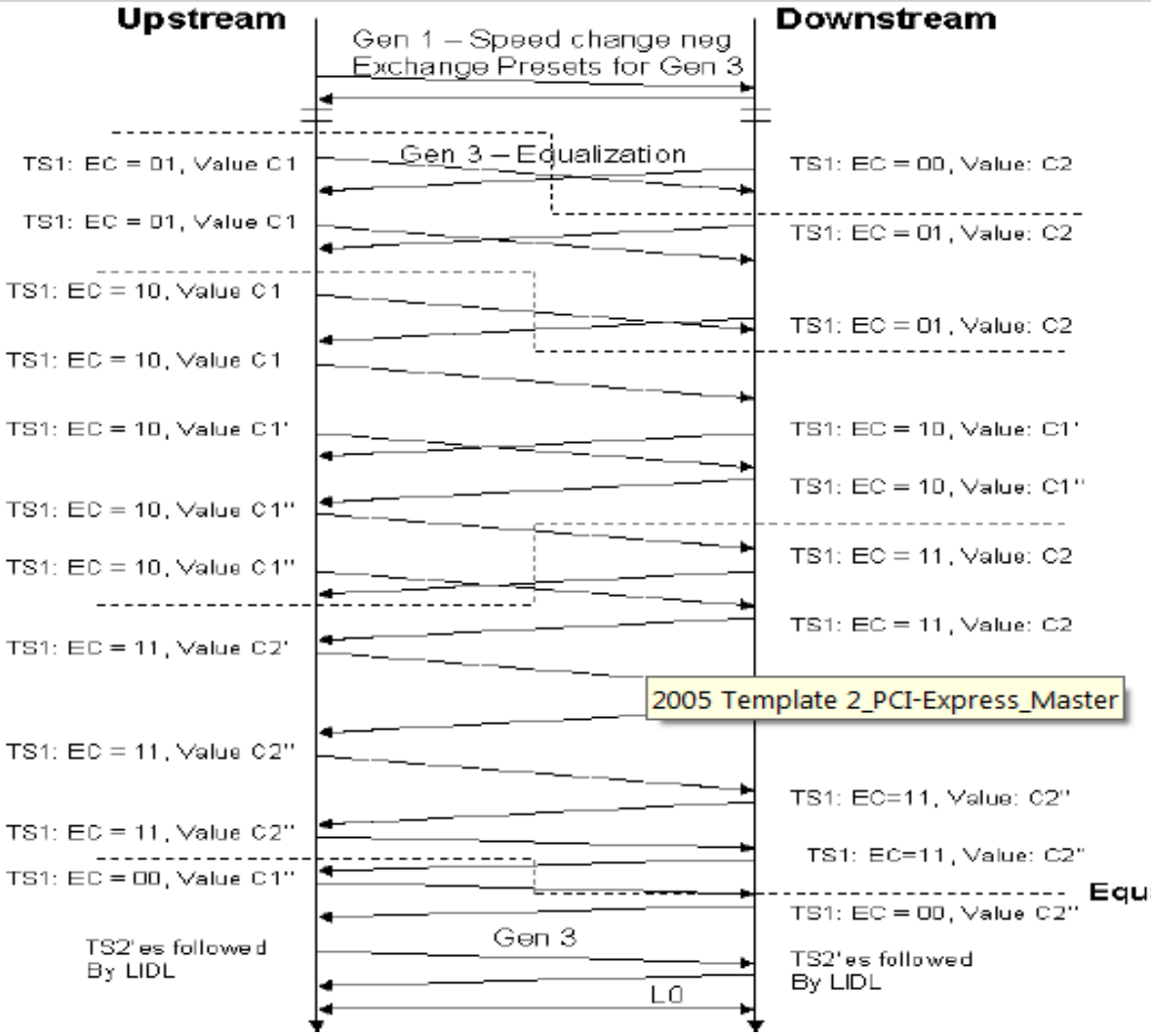
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8 Gig Dynamic Equalization



Phase 0: EQ TS2'es sent from USC (UpStream Component) to DownStream Component (DSC)

Phase 1: Both sides send the TS1'es and establish the link that is operational at a BER less than 10^{-4}.
EIEOS sent every 32 TS1'es

Phase 2: Downstream component requests upstream to set its transmitter's coefficients or presets such that it receives data at a BER less than or equal to 10^{-12}.
USC may send EIEOS every 65536 TS1'es on request from DSC. DSC sends EIEOS every 32 TS1'es.

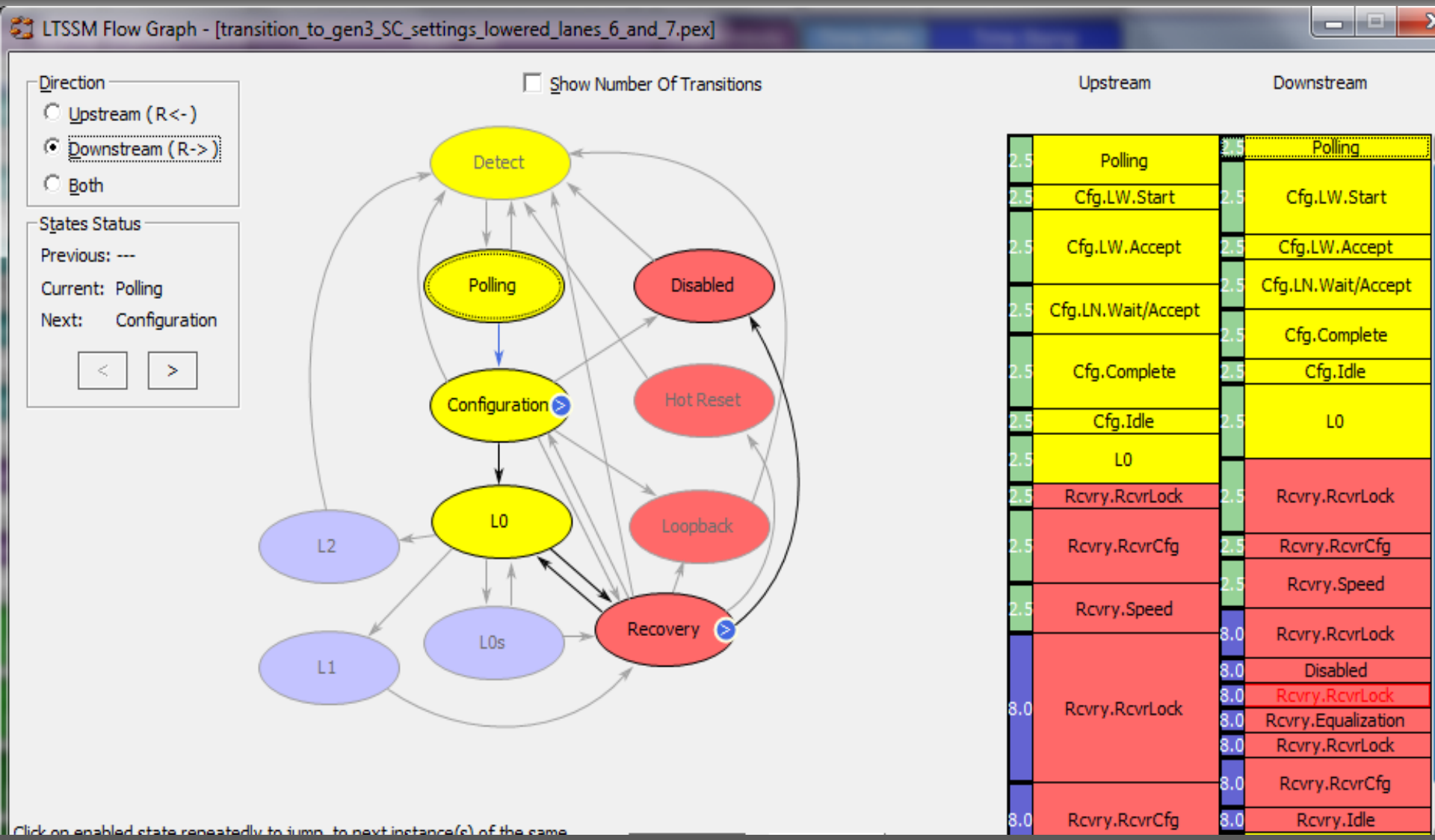
Phase 3: USC requests downstream to adjust its transmitter's coefficients or presets such that it receives data at a BER less than or equal to 10^{-12}.
DSC may send EIEOS every 65536 TS1'es on request from USC. USC sends EIEOS every 32 TS1'es.

Equalization Complete

Post Equalization:LTSSM goes through Recovery.RcvrLock, Recovery.RcvrCfg, Recovery.Idle to L0.
EIEOS sent after every 32 TS1/TS2'es

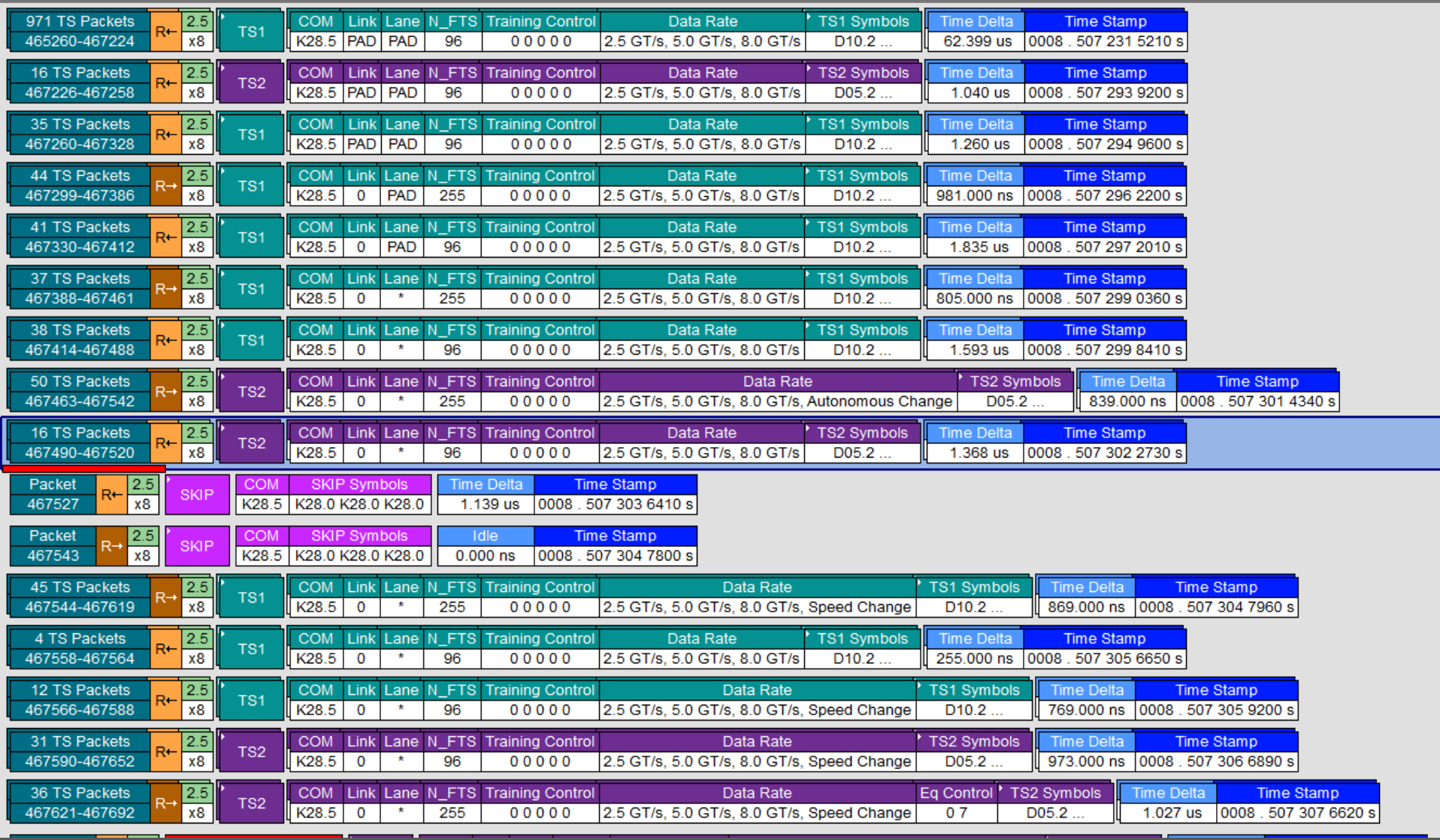
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LTSSM State Transition Diagram



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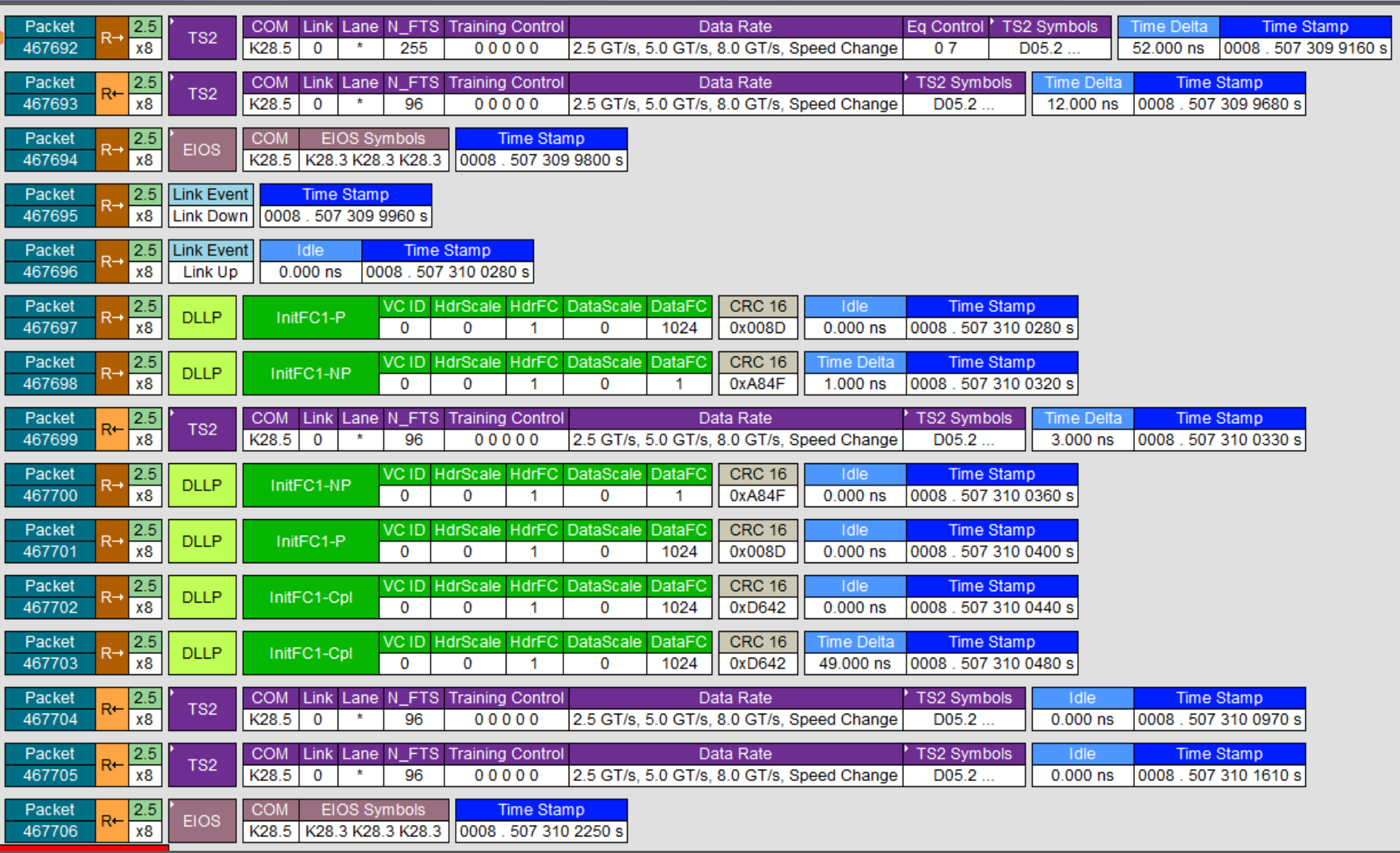
Initial Training with Autonomous Speed Change



971 TS Packets 465260-467224	R←	2.5 x8	TS1	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS1 Symbols	Time Delta	Time Stamp
				K28.5	PAD	PAD	96	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	D10.2 ...	62.399 us	0008 . 507 231 5210 s
16 TS Packets 467226-467258	R←	2.5 x8	TS2	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS2 Symbols	Time Delta	Time Stamp
				K28.5	PAD	PAD	96	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	D05.2 ...	1.040 us	0008 . 507 293 9200 s
35 TS Packets 467260-467328	R←	2.5 x8	TS1	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS1 Symbols	Time Delta	Time Stamp
				K28.5	PAD	PAD	96	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	D10.2 ...	1.260 us	0008 . 507 294 9600 s
44 TS Packets 467299-467386	R→	2.5 x8	TS1	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS1 Symbols	Time Delta	Time Stamp
				K28.5	0	PAD	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	D10.2 ...	981.000 ns	0008 . 507 296 2200 s
41 TS Packets 467330-467412	R←	2.5 x8	TS1	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS1 Symbols	Time Delta	Time Stamp
				K28.5	0	PAD	96	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	D10.2 ...	1.835 us	0008 . 507 297 2010 s
37 TS Packets 467388-467461	R→	2.5 x8	TS1	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS1 Symbols	Time Delta	Time Stamp
				K28.5	0	*	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	D10.2 ...	805.000 ns	0008 . 507 299 0360 s
38 TS Packets 467414-467488	R←	2.5 x8	TS1	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS1 Symbols	Time Delta	Time Stamp
				K28.5	0	*	96	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	D10.2 ...	1.593 us	0008 . 507 299 8410 s
50 TS Packets 467463-467542	R→	2.5 x8	TS2	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS2 Symbols	Time Delta	Time Stamp
				K28.5	0	*	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, Autonomous Change	D05.2 ...	839.000 ns	0008 . 507 301 4340 s
16 TS Packets 467490-467520	R←	2.5 x8	TS2	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS2 Symbols	Time Delta	Time Stamp
				K28.5	0	*	96	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	D05.2 ...	1.368 us	0008 . 507 302 2730 s
Packet 467527	R←	2.5 x8	SKIP	COM	SKIP Symbols			Time Delta	Time Stamp			
				K28.5	K28.0 K28.0 K28.0			1.139 us	0008 . 507 303 6410 s			
Packet 467543	R→	2.5 x8	SKIP	COM	SKIP Symbols			Idle	Time Stamp			
				K28.5	K28.0 K28.0 K28.0			0.000 ns	0008 . 507 304 7800 s			
45 TS Packets 467544-467619	R→	2.5 x8	TS1	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS1 Symbols	Time Delta	Time Stamp
				K28.5	0	*	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, Speed Change	D10.2 ...	869.000 ns	0008 . 507 304 7960 s
4 TS Packets 467558-467564	R←	2.5 x8	TS1	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS1 Symbols	Time Delta	Time Stamp
				K28.5	0	*	96	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	D10.2 ...	255.000 ns	0008 . 507 305 6650 s
12 TS Packets 467566-467588	R←	2.5 x8	TS1	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS1 Symbols	Time Delta	Time Stamp
				K28.5	0	*	96	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, Speed Change	D10.2 ...	769.000 ns	0008 . 507 305 9200 s
31 TS Packets 467590-467652	R←	2.5 x8	TS2	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS2 Symbols	Time Delta	Time Stamp
				K28.5	0	*	96	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, Speed Change	D05.2 ...	973.000 ns	0008 . 507 306 6890 s
36 TS Packets 467621-467692	R→	2.5 x8	TS2	COM	Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	TS2 Symbols	Time Delta	Time Stamp
				K28.5	0	*	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, Speed Change	0 7	D05.2 ...	1.027 us	0008 . 507 307 6620 s

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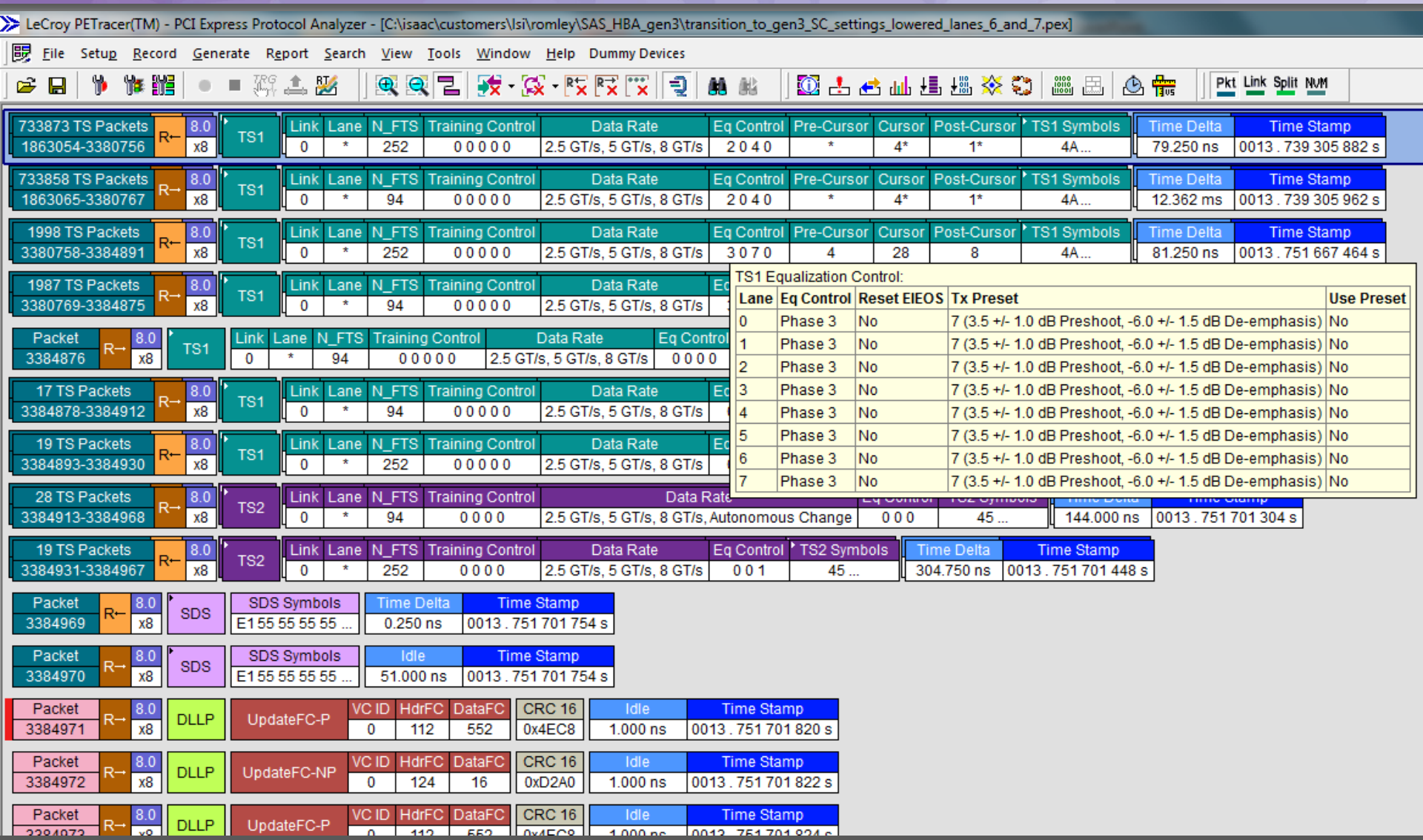
Transition to Recovery



Packet				COM	Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	TS2 Symbols	Time Delta	Time Stamp
467692	R→	2.5 x8	TS2	K28.5	0	*	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, Speed Change	0 7	D05.2 ...	52.000 ns	0008 . 507 309 9160 s
467693	R←	2.5 x8	TS2	K28.5	0	*	96	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, Speed Change		D05.2 ...	12.000 ns	0008 . 507 309 9680 s
467694	R→	2.5 x8	EIOS	COM	EIOS Symbols							Time Stamp	
				K28.5	K28.3 K28.3 K28.3							0008 . 507 309 9800 s	
467695	R→	2.5 x8	Link Event	Time Stamp									
			Link Down	0008 . 507 309 9960 s									
467696	R→	2.5 x8	Link Event	Idle	Time Stamp								
			Link Up	0.000 ns	0008 . 507 310 0280 s								
467697	R→	2.5 x8	DLLP	InitFC1-P	VC ID	HdrScale	HdrFC	DataScale	DataFC	CRC 16	Idle	Time Stamp	
					0	0	1	0	1024	0x008D	0.000 ns	0008 . 507 310 0280 s	
467698	R→	2.5 x8	DLLP	InitFC1-NP	VC ID	HdrScale	HdrFC	DataScale	DataFC	CRC 16	Time Delta	Time Stamp	
					0	0	1	0	1	0xA84F	1.000 ns	0008 . 507 310 0320 s	
467699	R←	2.5 x8	TS2	COM	Link	Lane	N_FTS	Training Control	Data Rate		TS2 Symbols	Time Delta	Time Stamp
				K28.5	0	*	96	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, Speed Change		D05.2 ...	3.000 ns	0008 . 507 310 0330 s
467700	R→	2.5 x8	DLLP	InitFC1-NP	VC ID	HdrScale	HdrFC	DataScale	DataFC	CRC 16	Idle	Time Stamp	
					0	0	1	0	1	0xA84F	0.000 ns	0008 . 507 310 0360 s	
467701	R→	2.5 x8	DLLP	InitFC1-P	VC ID	HdrScale	HdrFC	DataScale	DataFC	CRC 16	Idle	Time Stamp	
					0	0	1	0	1024	0x008D	0.000 ns	0008 . 507 310 0400 s	
467702	R→	2.5 x8	DLLP	InitFC1-Cpl	VC ID	HdrScale	HdrFC	DataScale	DataFC	CRC 16	Idle	Time Stamp	
					0	0	1	0	1024	0xD642	0.000 ns	0008 . 507 310 0440 s	
467703	R→	2.5 x8	DLLP	InitFC1-Cpl	VC ID	HdrScale	HdrFC	DataScale	DataFC	CRC 16	Time Delta	Time Stamp	
					0	0	1	0	1024	0xD642	49.000 ns	0008 . 507 310 0480 s	
467704	R←	2.5 x8	TS2	COM	Link	Lane	N_FTS	Training Control	Data Rate		TS2 Symbols	Idle	Time Stamp
				K28.5	0	*	96	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, Speed Change		D05.2 ...	0.000 ns	0008 . 507 310 0970 s
467705	R←	2.5 x8	TS2	COM	Link	Lane	N_FTS	Training Control	Data Rate		TS2 Symbols	Idle	Time Stamp
				K28.5	0	*	96	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, Speed Change		D05.2 ...	0.000 ns	0008 . 507 310 1610 s
467706	R←	2.5 x8	EIOS	COM	EIOS Symbols							Time Stamp	
				K28.5	K28.3 K28.3 K28.3							0008 . 507 310 2250 s	

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Transition to 8 Gig with Dynamic Equalization



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Dynamic Equalization Phase Transition Detailed Description

- Phase 2 and phase 3 transitions based on captures with server using a 12 gig SAS DUT
  - DS port sets EC = 0x10 in TS1 indicating to the downstream device transition to phase 2. In the trace this is happens in packet 783523.
  - US port sees this indication in packet 783532 and indicates it transitions to phase 2 by setting EC = 2 and desires to start equalization using presets rather than coefficients, by setting the use preset bit to 1, requesting preset 4.

Packet				Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
783531	R→	8.0 x8	TS1	0	*	94	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2070	6	43	13	4A...	16.250 ns	0013.730 513 274 s
Packet				Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
783532	R←	8.0 x8	TS1	0	*	252	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2041	4	28	8	4A...	0.000 ns	0013.730 513 290 s

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Dynamic Equalization Phase Transition Description

- The DS port (US device) transmitter will follow this request in packet 783547. It is advertising preset 7 and then transitions to preset 4 as requested by DS device

Packet				Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
783545	R→	8.0 x8	TS1	0	*	94	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2070	6	**	**	4A...	16.250 ns	0013.730 513 386 s
783546	R←	8.0 x8	TS1	0	*	252	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2041	4	28	8	4A...	0.000 ns	0013.730 513 402 s
783547	R→	8.0 x8	TS1	0	*	94	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2040	0	62	0	4A...	16.250 ns	0013.730 513 402 s

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Dynamic Equalization Phase Transition Description

- The DS device transmitter is now attempting to obtain block alignment based on preset 4 until packet 804011

Packet				Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
804009	R←	8.0 x8	TS1	0	0	252	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2041	4	28	8	4A 4A 4A 4A 4A 4A	0.250 ns	0013 . 730 680 066 s
				0	1	252	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2041	4	28	8	4A 4A 4A 4A 4A 4A		
				0	2	252	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2041	4	28	8	4A 4A 4A 4A 4A 4A		
				0	3	252	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2041	4	28	8	4A 4A 4A 4A 4A 08		
				0	4	252	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2041	4	28	8	4A 4A 4A 4A 20 08		
				0	5	252	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2041	4	28	8	4A 4A 4A 4A 4A 4A		
				0	6	252	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2041	4	28	8	4A 4A 4A 4A 4A 08		
				0	7	252	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2041	4	28	8	4A 4A 4A 4A 4A 4A		

- It is then switching to equalization by coefficients by setting the use preset bit to 0 and starting to gradually change coefficients waiting for the US device to follow.

Packet				Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
804010	R→	8.0 x8	TS1	0	0	94	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2040	0	62	0	4A 4A 4A 4A 4A 08	16.000 ns	0013 . 730 680 066 s
				0	1	94	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2040	0	62	0	4A 4A 4A 4A 4A 4A		
				0	2	94	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2040	0	62	0	4A 4A 4A 4A 4A 4A		
				0	3	94	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2040	0	62	0	4A 4A 4A 4A 4A 4A		
				0	4	94	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2040	0	62	0	4A 4A 4A 4A 4A 4A		
				0	5	94	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2040	0	62	0	4A 4A 4A 4A 4A 08		
				0	6	94	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2040	0	62	0	4A 4A 4A 4A 4A F7		
				0	7	94	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2040	0	62	0	4A 4A 4A 4A 4A 08		

- At packet 804011 the DS device starts varying some of the coefficients for some of the lanes moving to fine tune with use preset flag set to 0.

Packet				Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
804011	R←	8.0 x8	TS1	0	0	252	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2040	0	60	2	4A 4A 4A 4A 4A 4A	0.250 ns	0013 . 730 680 082 s
				0	1	252	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2040	0	62	0	4A 4A 4A 4A 4A 4A		
				0	2	252	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2040	0	60	2	4A 4A 4A 4A 4A 4A		
				0	3	252	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2040	0	60	2	4A 4A 4A 4A 4A 4A		
				0	4	252	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2040	0	60	2	4A 4A 4A 4A 20 08		
				0	5	252	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2040	0	60	2	4A 4A 4A 4A 4A F7		
				0	6	252	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2040	0	60	2	4A 4A 4A 4A 4A 4A		
				0	7	252	00000	2.5 GT/s, 5 GT/s, 8 GT/s	2040	0	60	2	4A 4A 4A 4A 4A 4A		

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Dynamic Equalization Phase Transition Description

Packet			
804015	R←	8.0	x8

TS1

Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
0	0	252	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 4 0	0	60	2	4A 4A 4A 4A 4A 4A	0.250 ns	0013 . 730 680 114 s
0	1	252	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 4 0	0	62	0	4A 4A 4A 4A 20 08		
0	2	252	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 4 0	0	60	2	4A 4A 4A 4A 4A 4A		
0	3	252	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 4 0	0	60	2	4A 4A 4A 4A 4A 4A		
0	4	252	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 4 0	0	60	2	4A 4A 4A 4A 4A 4A		
0	5	252	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 4 0	0	60	2	4A 4A 4A 4A 4A 4A		
0	6	252	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 4 0	0	60	2	4A 4A 4A 4A 4A 4A		
0	7	252	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 4 0	0	60	2	4A 4A 4A 4A 4A 4A		

- The DS device follows here

Packet			
804016	R→	8.0	x8

TS1

Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Idle	Time Stamp
0	0	94	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 4 0	0	62	0	4A 4A 4A 4A 20 08	0.000 ns	0013 . 730 680 114 s
0	1	94	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 4 0	0	62	0	4A 4A 4A 4A 4A 4A		
0	2	94	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 4 0	0	62	0	4A 4A 4A 4A 4A 4A		
0	3	94	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 4 0	0	62	0	4A 4A 4A 4A 4A 08		
0	4	94	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 4 0	0	62	0	4A 4A 4A 4A 4A 4A		
0	5	94	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 4 0	0	62	0	4A 4A 4A 4A 4A 4A		
0	6	94	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 4 0	0	62	0	4A 4A 4A 4A 4A 4A		
0	7	94	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 4 0	0	62	0	4A 4A 4A 4A 4A 08		

- This process continues per coefficient

Packet			
804017	R→	8.0	x8

TS1

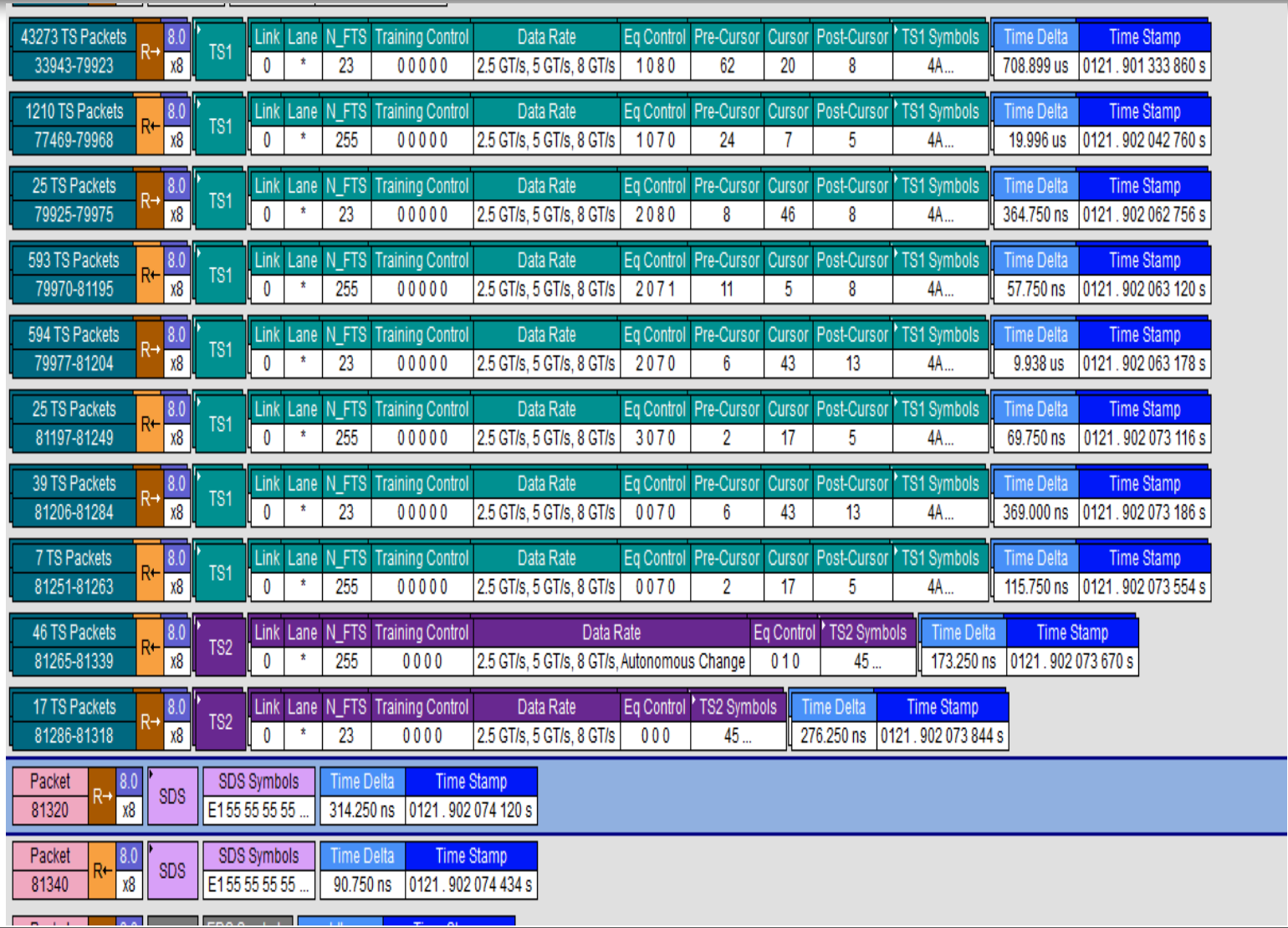
Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
0	0	94	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 4 0	0	60	2	4A 4A 4A 4A 4A 08	1.750 ns	0013 . 730 680 128 s
0	1	94	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 4 0	0	62	0	4A 4A 4A 4A 4A 4A		
0	2	94	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 4 0	0	60	2	4A 4A 4A 4A 4A 4A		
0	3	94	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 4 0	0	60	2	4A 4A 4A 4A 4A 08		
0	4	94	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 4 0	0	60	2	4A 4A 4A 4A 4A 08		
0	5	94	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 4 0	0	60	2	4A 4A 4A 4A 4A 4A		
0	6	94	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 4 0	0	60	2	4A 4A 4A 4A 4A 4A		
0	7	94	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 4 0	0	60	2	4A 4A 4A 4A 4A 4A		

- Similarly going into phase 3.

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Dynamic Equalization Phase Transition Description

- This platform varies presets in phase 2 only
- Phase 3 does not require equalization



43273 TS Packets 33943-79923	R→	8.0 x8	TS1	Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
				0	*	23	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	1 0 8 0	62	20	8	4A...	708.899 us	0121 . 901 333 860 s
1210 TS Packets 77469-79968	R←	8.0 x8	TS1	Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
				0	*	255	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	1 0 7 0	24	7	5	4A...	19.996 us	0121 . 902 042 760 s
25 TS Packets 79925-79975	R→	8.0 x8	TS1	Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
				0	*	23	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 8 0	8	46	8	4A...	364.750 ns	0121 . 902 062 756 s
593 TS Packets 79970-81195	R←	8.0 x8	TS1	Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
				0	*	255	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 7 1	11	5	8	4A...	57.750 ns	0121 . 902 063 120 s
594 TS Packets 79977-81204	R→	8.0 x8	TS1	Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
				0	*	23	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	2 0 7 0	6	43	13	4A...	9.938 us	0121 . 902 063 178 s
25 TS Packets 81197-81249	R←	8.0 x8	TS1	Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
				0	*	255	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	3 0 7 0	2	17	5	4A...	69.750 ns	0121 . 902 073 116 s
39 TS Packets 81206-81284	R→	8.0 x8	TS1	Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
				0	*	23	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	0 0 7 0	6	43	13	4A...	369.000 ns	0121 . 902 073 186 s
7 TS Packets 81251-81263	R←	8.0 x8	TS1	Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
				0	*	255	0 0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	0 0 7 0	2	17	5	4A...	115.750 ns	0121 . 902 073 554 s
46 TS Packets 81265-81339	R←	8.0 x8	TS2	Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	TS2 Symbols				Time Delta	Time Stamp
				0	*	255	0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s, Autonomous Change	0 1 0	45 ...				173.250 ns	0121 . 902 073 670 s
17 TS Packets 81286-81318	R→	8.0 x8	TS2	Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	TS2 Symbols				Time Delta	Time Stamp
				0	*	23	0 0 0 0	2.5 GT/s, 5 GT/s, 8 GT/s	0 0 0	45 ...				276.250 ns	0121 . 902 073 844 s
Packet 81320	R→	8.0 x8	SDS	SDS Symbols			Time Delta	Time Stamp							
				E1 55 55 55 55 ...			314.250 ns	0121 . 902 074 120 s							
Packet 81340	R←	8.0 x8	SDS	SDS Symbols			Time Delta	Time Stamp							
				E1 55 55 55 55 ...			90.750 ns	0121 . 902 074 434 s							

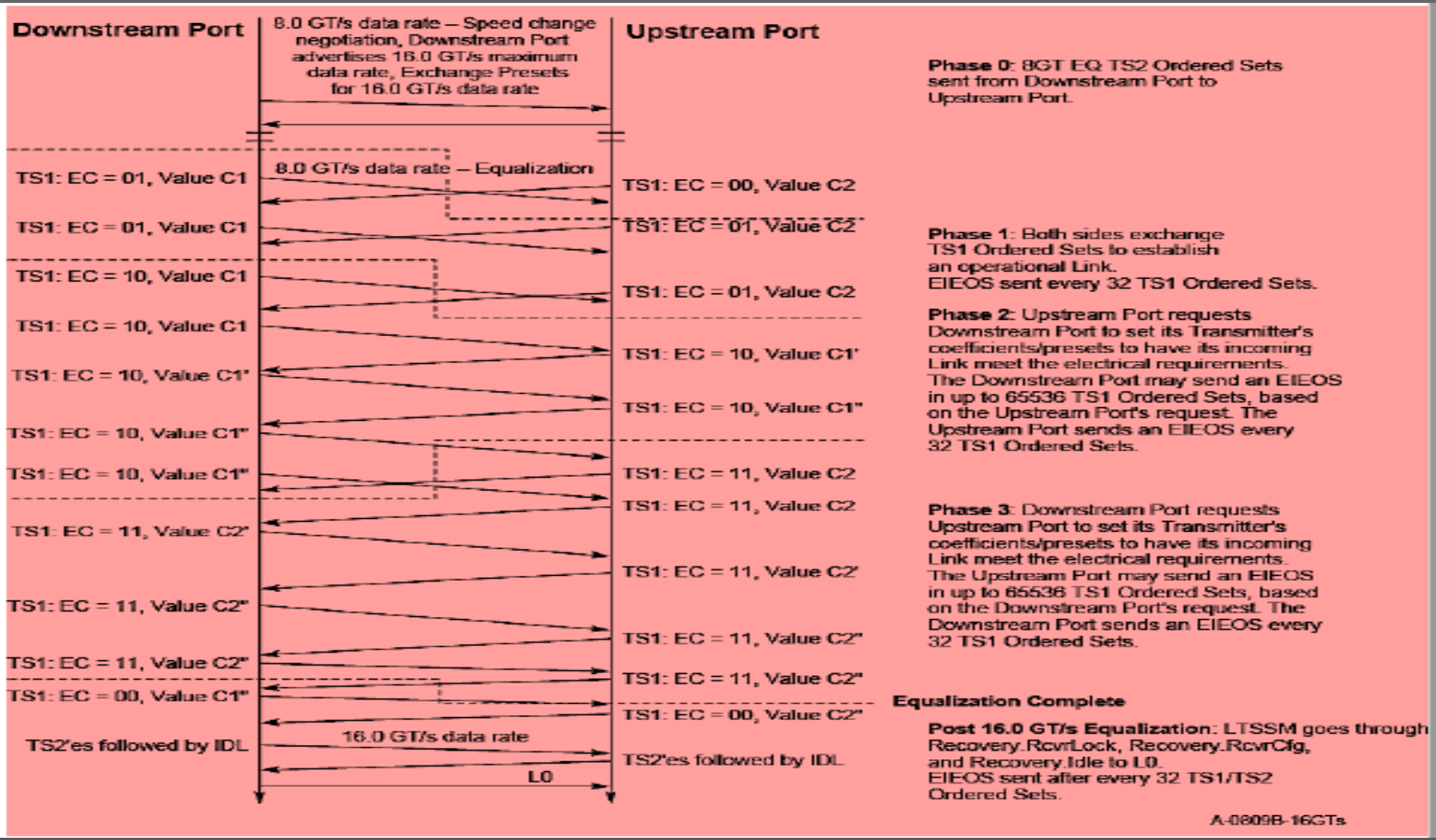
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Agenda

- Introduction
- Initial Training Analysis
- Transmitter and Receiver Equalization
- 8 Gig Speed Transition
- **16 Gig Speed Transition**
- Violations Detected by PCI-SIG Compliance
- Violations Detected by Additional Validation Tests
- Automation of a Validation Test Suite
- Summary

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16 Gig Transition Rules



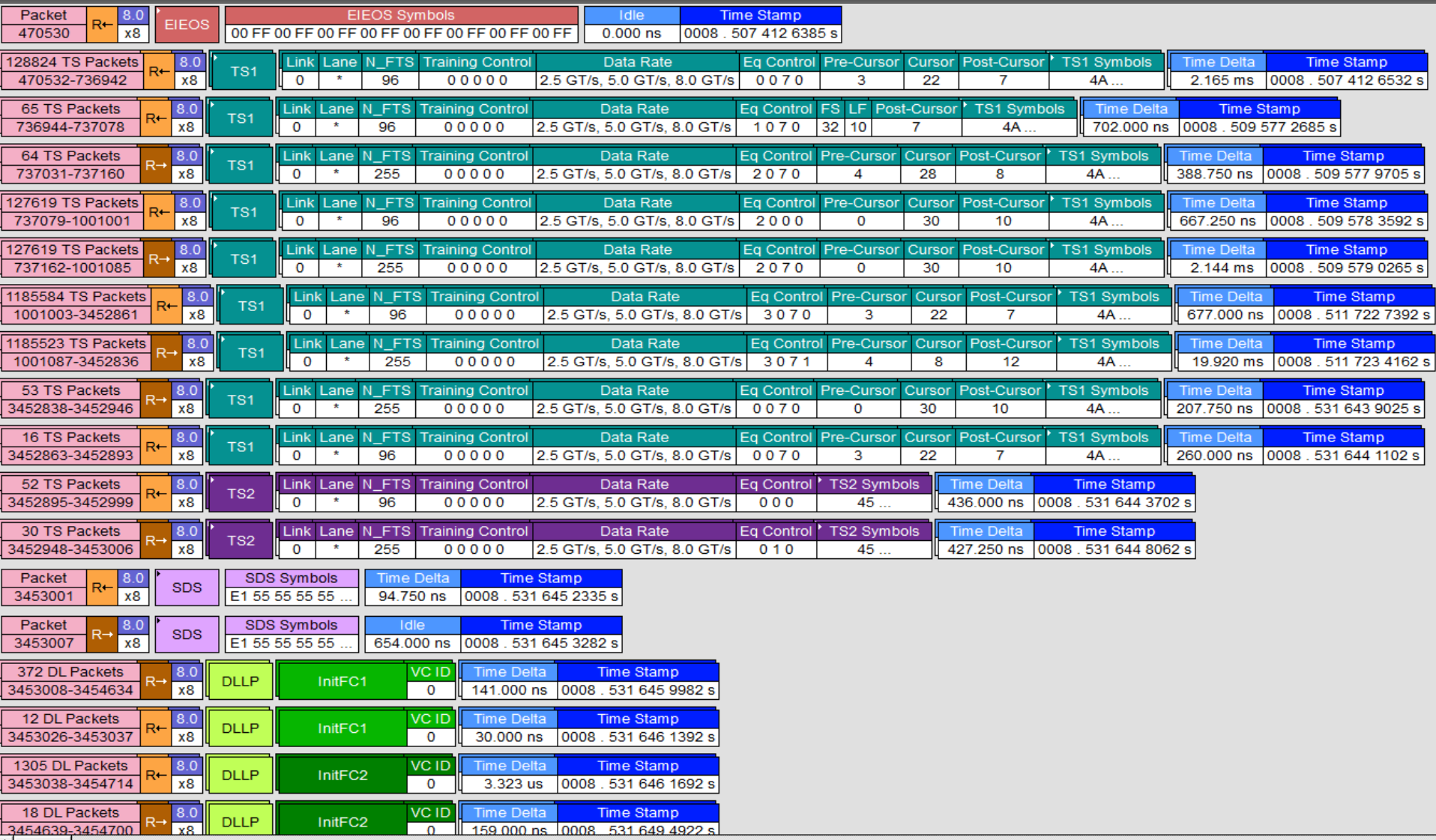
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16 Gig Transition Rules

- 16 GT/s EQ only after 8 GT/s EQ has successfully completed
  - DSP withholds advertising 16 GT/s Data Rate in Recovery until 8 GT/s EQ has successfully completed
- A Port may use a different preset in its Tx than it requests its Link Partner to use
  - Preset values (for both ports) come from the Downstream Port's (HwInit) CSR (USP's request, if implemented, is implementation specific)
- The DS Port may redo 8 GT/s equalization prior to proceeding to the 16 GT/s equalization procedure in the following cases:
  - DS Port detects 8 GT/s equalization problems
  - US Port made an 8 GT/s equalization redo request (by setting the Request Equalization bit to 1b and the Equalization Request Data Rate to 0b in the TS2s it sent in Recovery.RcvrCfg)

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First Transition to 8 Gig with Dynamic Equalization



Packet			EIEOS	EIEOS Symbols	Idle	Time Stamp
470530	R←	8.0 x8		00 FF 00 FF 00 FF 00 FF 00 FF 00 FF 00 FF 00 FF	0.000 ns	0008 . 507 412 6385 s

				Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
128824 TS Packets 470532-736942	R←	8.0 x8	TS1	0	*	96	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	0 0 7 0	3	22	7	4A ...	2.165 ms	0008 . 507 412 6532 s
65 TS Packets 736944-737078	R←	8.0 x8	TS1	0	*	96	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	1 0 7 0	32	10	7	4A ...	702.000 ns	0008 . 509 577 2685 s
64 TS Packets 737031-737160	R→	8.0 x8	TS1	0	*	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	2 0 7 0	4	28	8	4A ...	388.750 ns	0008 . 509 577 9705 s
127619 TS Packets 737079-1001001	R←	8.0 x8	TS1	0	*	96	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	2 0 0 0	0	30	10	4A ...	667.250 ns	0008 . 509 578 3592 s
127619 TS Packets 737162-1001085	R→	8.0 x8	TS1	0	*	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	2 0 7 0	0	30	10	4A ...	2.144 ms	0008 . 509 579 0265 s
1185584 TS Packets 1001003-3452861	R←	8.0 x8	TS1	0	*	96	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 7 0	3	22	7	4A ...	677.000 ns	0008 . 511 722 7392 s
1185523 TS Packets 1001087-3452836	R→	8.0 x8	TS1	0	*	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 7 1	4	8	12	4A ...	19.920 ms	0008 . 511 723 4162 s
53 TS Packets 3452838-3452946	R→	8.0 x8	TS1	0	*	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	0 0 7 0	0	30	10	4A ...	207.750 ns	0008 . 531 643 9025 s
16 TS Packets 3452863-3452893	R←	8.0 x8	TS1	0	*	96	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	0 0 7 0	3	22	7	4A ...	260.000 ns	0008 . 531 644 1102 s

				Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	TS2 Symbols	Time Delta	Time Stamp
52 TS Packets 3452895-3452999	R→	8.0 x8	TS2	0	*	96	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	0 0 0	45 ...	436.000 ns	0008 . 531 644 3702 s
30 TS Packets 3452948-3453006	R→	8.0 x8	TS2	0	*	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	0 1 0	45 ...	427.250 ns	0008 . 531 644 8062 s

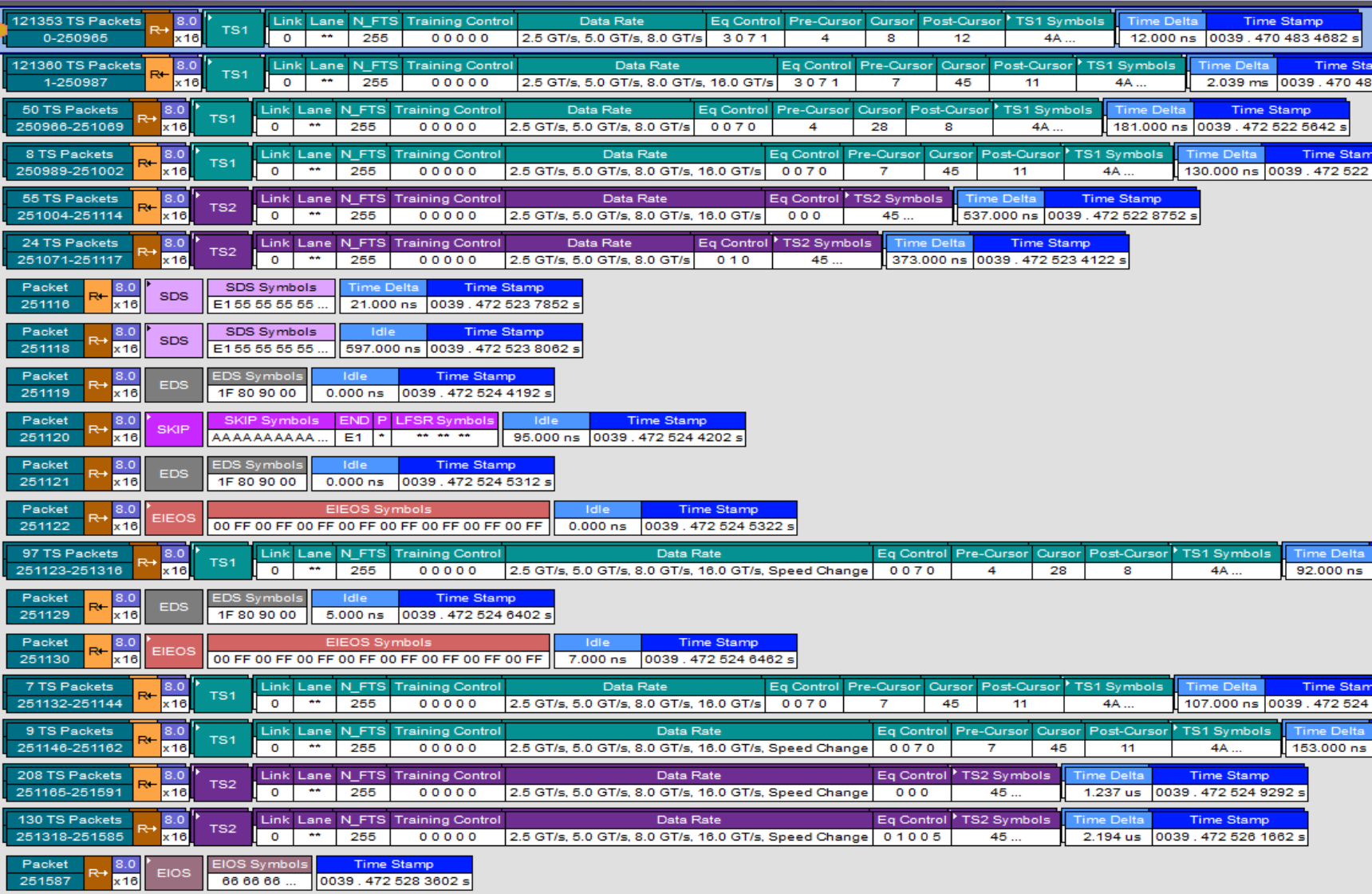
Packet			SDS	SDS Symbols	Time Delta	Time Stamp
3453001	R←	8.0 x8	SDS	E1 55 55 55 55 ...	94.750 ns	0008 . 531 645 2335 s

Packet			SDS	SDS Symbols	Idle	Time Stamp
3453007	R→	8.0 x8	SDS	E1 55 55 55 55 ...	654.000 ns	0008 . 531 645 3282 s

					VC ID	Time Delta	Time Stamp
372 DL Packets 3453008-3454634	R→	8.0 x8	DLLP	InitFC1	0	141.000 ns	0008 . 531 645 9982 s
12 DL Packets 3453026-3453037	R←	8.0 x8	DLLP	InitFC1	0	30.000 ns	0008 . 531 646 1392 s
1305 DL Packets 3453038-3454714	R←	8.0 x8	DLLP	InitFC2	0	3.323 us	0008 . 531 646 1692 s
18 DL Packets 3454639-3454700	R→	8.0 x8	DLLP	InitFC2	0	159.000 ns	0008 . 531 649 4922 s

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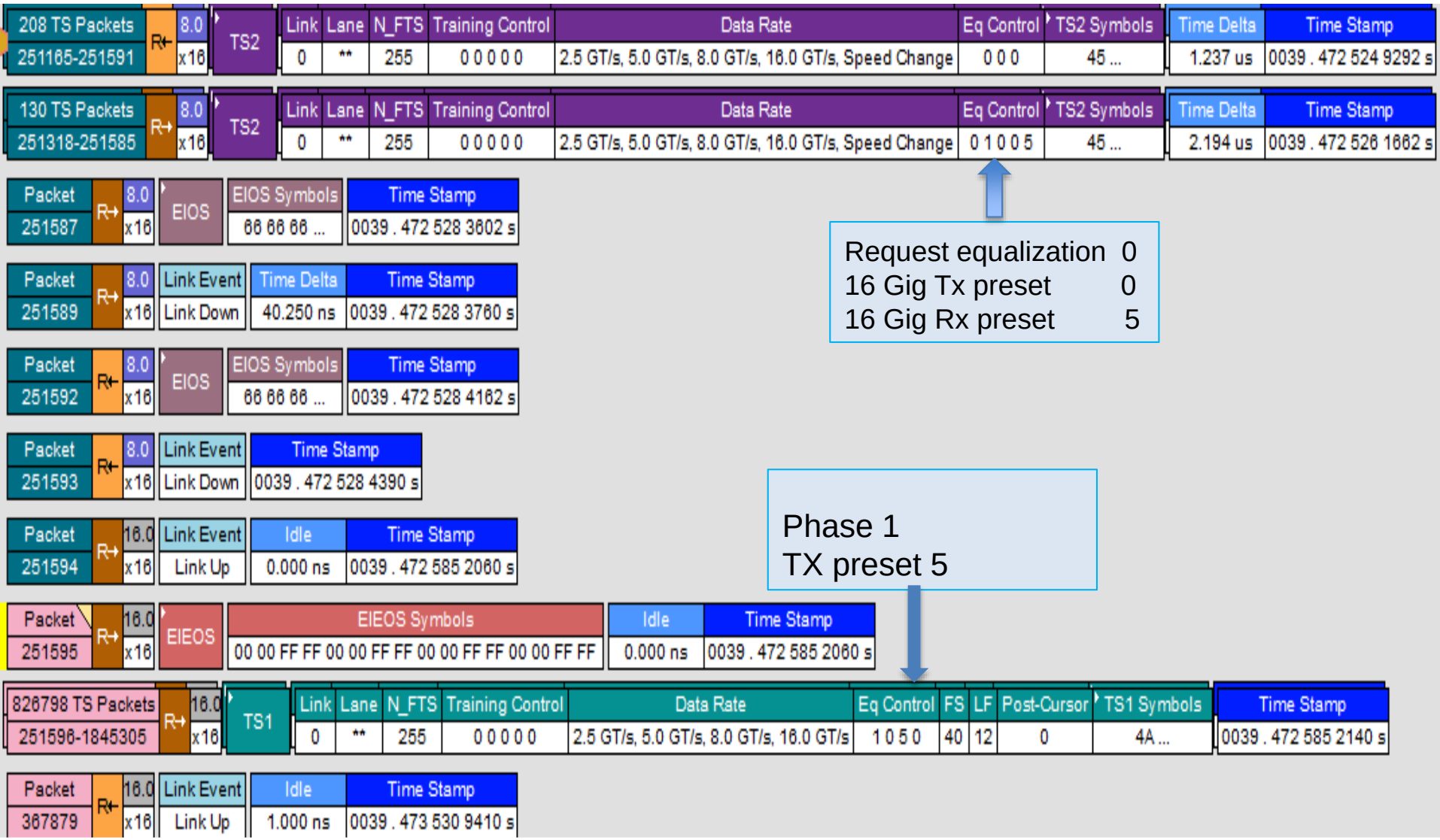
Second Transition to 8 Gig Before Transition to 16 Gig



121353 TS Packets 0-250965	R↔	8.0 x16	TS1	Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
				0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 7 1	4	8	12	4A ...	12.000 ns	0039 . 470 483 4682 s
121360 TS Packets 1-250987	R↔	8.0 x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 7 1	7	45	11	4A ...	2.039 ms	0039 . 470 483 4802 s
50 TS Packets 250966-251069	R↔	8.0 x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	0 0 7 0	4	28	8	4A ...	181.000 ns	0039 . 472 522 5642 s
8 TS Packets 250989-251002	R↔	8.0 x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	0 0 7 0	7	45	11	4A ...	130.000 ns	0039 . 472 522 7452 s
55 TS Packets 251004-251114	R↔	8.0 x16	TS2	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	0 0 0	45 ...				537.000 ns	0039 . 472 522 8752 s
24 TS Packets 251071-251117	R↔	8.0 x16	TS2	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	0 1 0	45 ...				373.000 ns	0039 . 472 523 4122 s
Packet 251116	R↔	8.0 x16	SDS	SDS Symbols					Time Delta						Time Stamp
				E1 55 55 55 55 ...					21.000 ns						0039 . 472 523 7852 s
Packet 251118	R↔	8.0 x16	SDS	SDS Symbols					Idle						Time Stamp
				E1 55 55 55 55 ...					597.000 ns						0039 . 472 523 8062 s
Packet 251119	R↔	8.0 x16	EDS	EDS Symbols					Idle						Time Stamp
				1F 80 90 00					0.000 ns						0039 . 472 524 4192 s
Packet 251120	R↔	8.0 x16	SKIP	SKIP Symbols		END	P	LFSR Symbols						Idle	Time Stamp
				AAAAAAAAAA ...		E1	*	** ** **						95.000 ns	0039 . 472 524 4202 s
Packet 251121	R↔	8.0 x16	EDS	EDS Symbols					Idle						Time Stamp
				1F 80 90 00					0.000 ns						0039 . 472 524 5312 s
Packet 251122	R↔	8.0 x16	EIEOS	EIEOS Symbols										Idle	Time Stamp
				00 FF 00 FF 00 FF 00 FF 00 FF 00 FF 00 FF										0.000 ns	0039 . 472 524 5322 s
97 TS Packets 251123-251316	R↔	8.0 x16	TS1	Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
				0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s, Speed Change	0 0 7 0	4	28	8	4A ...	92.000 ns	0039 . 472 524 5482 s
Packet 251129	R↔	8.0 x16	EDS	EDS Symbols					Idle						Time Stamp
				1F 80 90 00					5.000 ns						0039 . 472 524 6402 s
Packet 251130	R↔	8.0 x16	EIEOS	EIEOS Symbols										Idle	Time Stamp
				00 FF 00 FF 00 FF 00 FF 00 FF 00 FF 00 FF										7.000 ns	0039 . 472 524 6462 s
7 TS Packets 251132-251144	R↔	8.0 x16	TS1	Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
				0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	0 0 7 0	7	45	11	4A ...	107.000 ns	0039 . 472 524 6692 s
9 TS Packets 251146-251162	R↔	8.0 x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s, Speed Change	0 0 7 0	7	45	11	4A ...	153.000 ns	0039 . 472 524 7762 s
208 TS Packets 251165-251591	R↔	8.0 x16	TS2	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s, Speed Change	0 0 0	45 ...				1.237 us	0039 . 472 524 9292 s
130 TS Packets 251318-251585	R↔	8.0 x16	TS2	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s, Speed Change	0 1 0 0 5	45 ...				2.194 us	0039 . 472 526 1662 s
Packet 251587	R↔	8.0 x16	EIOS	EIOS Symbols											Time Stamp
				66 66 66 ...											0039 . 472 528 3602 s

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Recovery Before 16 Gig Speed Change



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16 Gig EQ: Phase 3 Individual Lane Presets Adjustments

2371045 TS Packets	R→	16.0	TS1
8986625-13890120		x16	

Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 7 1	4	8	12	4A ...	171.000 ns	0039 . 508 543 2040 s

Packet	R←	16.0	TS1
8986666		x16	

Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Idle	Time Stamp
0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A	0.000 ns	0039 . 508 543 3750 s
0	1	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	2	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	3	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	4	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	5	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	6	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	7	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	8	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	9	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	10	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 7 1	7	45	11	4A 4A 4A 4A 4A 4A		
0	11	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	12	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	13	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	14	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	15	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		

Packet	R←	16.0	TS1
8986667		x16	

Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A	16.000 ns	0039 . 508 543 3780 s
0	1	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	2	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	3	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	4	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	5	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	6	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	7	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	8	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	9	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	10	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 7 1	7	45	11	4A 4A 4A 4A 4A 4A		
0	11	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	12	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	13	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 7 1	7	45	11	4A 4A 4A 4A 4A 4A		
0	14	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		
0	15	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A		

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16 Gig EQ: Phase 3 Individual Lane Presets Adjustments

Packet	R←	16.0	TS1
8986667		x16	

Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols
0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	1	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	2	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	3	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	4	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	5	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	6	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	7	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	8	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	9	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	10	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 7 1	7	45	11	4A 4A 4A 4A 4A 4A
0	11	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	12	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	13	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 7 1	7	45	11	4A 4A 4A 4A 4A 4A
0	14	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	15	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A

Time Delta	Time Stamp
16.000 ns	0039 . 508 543 3780 s

3 TS Packets	R←	16.0	TS1
8986671-8986675		x16	

Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols
0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	1	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	2	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	3	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	4	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 7 1	7	45	11	4A 4A 4A 4A 4A 4A
0	5	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	6	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	7	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	8	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	9	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	10	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 7 1	7	45	11	4A 4A 4A 4A 4A 4A
0	11	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	12	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	13	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 7 1	7	45	11	4A 4A 4A 4A 4A 4A
0	14	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A
0	15	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6	57	0	4A 4A 4A 4A 4A 4A

Time Delta	Time Stamp
24.000 ns	0039 . 508 543 3940 s

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16 Gig EQ: Phase 3 Individual Lane Presets Adjustments

Packet	Dir	Rate	Width	Type	Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	FS	LF	Cursor	Post-Cursor	Reject	TS1 Symbols	Time Delta / Idle	Time Stamp
701817 TS Packets 393807-1845215	R←	16.0	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	0 0 5 0	6			57	0		4A ...	Time Delta 5.896 ms	0039 . 473 634 8700 s
714440 TS Packets 1845217-3322731	R←	16.0	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	1 0 5 0		63	21		0		4A ...	Time Delta 367.000 ns	0039 . 479 531 2250 s
714439 TS Packets 1845308-3322817	R→	16.0	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	2 0 5 0	4			36	0		4A ...	Time Delta 6.002 ms	0039 . 479 531 5920 s
2738685 TS Packets 3322732-8986533	R←	16.0	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	2 0 5 0	4			36	0		4A ...	Time Delta 352.000 ns	0039 . 485 533 6280 s
Packet 3322819	R→	16.0	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	2 0 5 0	7			45	11	1	4A ...	Idle 0.000 ns	0039 . 485 533 9800 s
2738685 TS Packets 3322821-8986623	R→	16.0	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	2 0 5 0	4			36	0		4A ...	Time Delta 23.009 ms	0039 . 485 533 9880 s
63 TS Packets 8986536-8986663	R←	16.0	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 5 0	6			57	0		4A ...	Time Delta 361.000 ns	0039 . 508 542 8430 s
2371045 TS Packets 8986625-13890120	R→	16.0	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 7 1	4			8	12		4A ...	Time Delta 171.000 ns	0039 . 508 543 2040 s
Packet 8986666	R←	16.0	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 * *	*			**	**		4A ...	Idle 0.000 ns	0039 . 508 543 3750 s
Packet 8986667	R←	16.0	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 * *	*			**	**		4A ...	Time Delta 16.000 ns	0039 . 508 543 3780 s
3 TS Packets 8986671-8986675	R←	16.0	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 * *	*			**	**		4A ...	Time Delta 24.000 ns	0039 . 508 543 3940 s
Packet 8986677	R←	16.0	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 * *	*			**	**		4A ...	Idle 1.000 ns	0039 . 508 543 4180 s
Packet 8986680	R←	16.0	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 * *	*			**	**		4A ...	Time Delta 17.000 ns	0039 . 508 543 4270 s
3 TS Packets 8986684-8986687	R←	16.0	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 * *	*			**	**		4A ...	Time Delta 23.000 ns	0039 . 508 543 4440 s
Packet 8986690	R←	16.0	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 * *	*			**	**		4A ...	Idle 1.000 ns	0039 . 508 543 4670 s
Packet 8986692	R←	16.0	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 * *	*			**	**		4A ...	Time Delta 17.000 ns	0039 . 508 543 4760 s
3 TS Packets 8986696-8986700	R←	16.0	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 * *	*			**	**		4A ...	Time Delta 23.000 ns	0039 . 508 543 4930 s
Packet 8986702	R←	16.0	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 * *	*			**	**		4A ...	Idle 0.000 ns	0039 . 508 543 5160 s
2 TS Packets 8986704-8986708	R←	16.0	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 * *	*			**	**		4A ...	Time Delta 24.000 ns	0039 . 508 543 5240 s
Packet 8986710	R←	16.0	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 * *	*			**	**		4A ...	Time Delta 23.000 ns	0039 . 508 543 5480 s

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16 Gig Equalization Complete

3 TS Packets		16.0		Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
8986696-8986700	R←	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 * *	*	**	**	4A ...	23.000 ns	0039 . 508 543 4930 s

Packet		16.0		Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Idle	Time Stamp
8986702	R←	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 * *	*	**	**	4A ...	0.000 ns	0039 . 508 543 5160 s

2 TS Packets		16.0		Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
8986704-8986708	R←	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 * *	*	**	**	4A ...	24.000 ns	0039 . 508 543 5240 s

Packet		16.0		Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
8986710	R←	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 * *	*	**	**	4A ...	23.000 ns	0039 . 508 543 5480 s

2201911 TS Packets		16.0		Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
8986715-13540428	R←	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 7 1	7	45	11	4A ...	18.499 ms	0039 . 508 543 5710 s

Packet		16.0	Training Sequence Error		Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Idle	Time Stamp
13540430	R←	x16	TSFormatErr	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 7 1	7	45	11	4A ...	0.000 ns	0039 . 527 043 0440 s

169102 TS Packets		16.0		Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
13540432-13890149	R←	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	3 0 7 1	7	45	11	4A ...	1.421 ms	0039 . 527 043 0520 s

56 TS Packets		16.0		Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
13890122-13890238	R→	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	0 0 5 0	4	36	0	4A ...	120.000 ns	0039 . 528 463 6620 s

8 TS Packets		16.0		Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta	Time Stamp
13890151-13890165	R←	x16	TS1	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	0 0 7 0	7	45	11	4A ...	64.000 ns	0039 . 528 463 7820 s

62 TS Packets		16.0		Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	TS2 Symbols	Time Delta	Time Stamp
13890167-13890290	R←	x16	TS2	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	0 0 0	45 ...	304.000 ns	0039 . 528 463 8460 s

27 TS Packets		16.0		Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	TS2 Symbols	Time Delta	Time Stamp
13890240-13890291	R→	x16	TS2	0	**	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, 16.0 GT/s	0 1 0	45 ...	210.000 ns	0039 . 528 464 1500 s

Packet		16.0		SKIP Symbols	END	P	FR	SR	CRC	MP	UM	MT	RN	Payload	Idle	Time Stamp
13890292	R←	x16	SKIP	AAAAAAAAAA ...	78	0	0	0	0	0	0	7	0	156	0.000 ns	0039 . 528 464 3600 s

Packet		16.0		SDS Symbols	Time Delta	Time Stamp
13890293	R←	x16	SDS	E1 55 55 55 55 ...	0.000 ns	0039 . 528 464 3660 s

Packet		16.0		SKIP Symbols	END	P	FR	SR	CRC	MP	UM	MT	RN	Payload	Idle	Time Stamp
13890294	R→	x16	SKIP	AAAAAAAAAA ...	78	0	0	0	0	0	0	3	1	56	0.000 ns	0039 . 528 464 3660 s

Packet		16.0		SDS Symbols	Idle	Time Stamp
13890295	R→	x16	SDS	E1 55 55 55 55 ...	8.000 ns	0039 . 528 464 3740 s

129 DL Packets		16.0			VC ID	Time Delta	Time Stamp
13890296-13890613	R→	x16	DLLP	InitFC1	0	91.000 ns	0039 . 528 464 3900 s

159 DL Packets		16.0			VC ID	Time Delta	Time Stamp
13890299-13890529	R←	x16	DLLP	InitFC1	0	401.000 ns	0039 . 528 464 4810 s

69 DL Packets		16.0			VC ID	Time Delta	Time Stamp
13890533-13890673	R←	x16	DLLP	InitFC2	0	76.000 ns	0039 . 528 464 8820 s

84 DL Packets		16.0			VC ID	Time Delta	Time Stamp
13890615-13890736	R→	x16	DLLP	InitFC2	0	854.500 ns	0039 . 528 464 9580 s

Packet		16.0		EDS Symbols	Idle	Time Stamp
13890737	R←	x16	EDS	1F 80 90 00	4.000 ns	0039 . 528 465 8125 s

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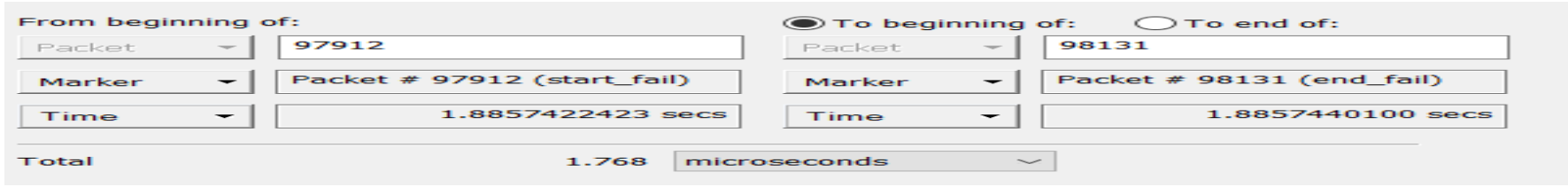
Agenda

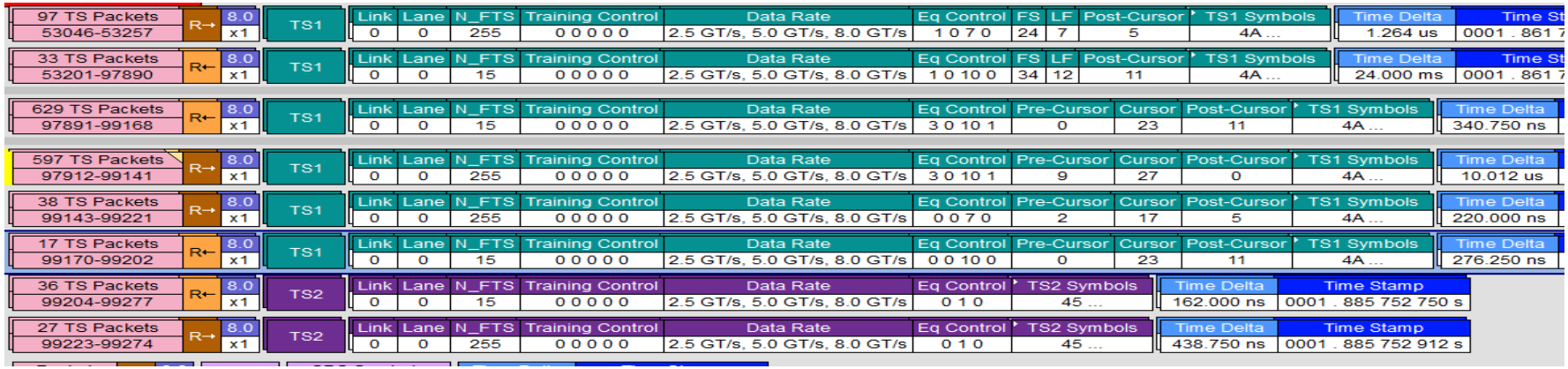
- Introduction
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Adjusting Presets and Adjusting Coefficient Tests

- Although phase transitions are correct device can fail the time limits of these tests
  - For adjusting presets device accepting preset expected to take less than 1 usec but taking 1.9 usec.
  - For adjusting coefficients the test expects device to accept within 1 usec and it takes 2.3 usec.

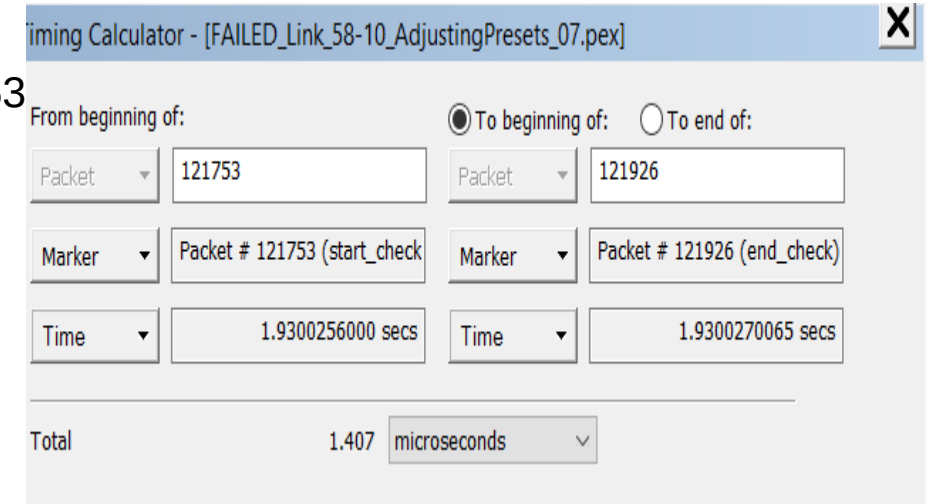




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Adjusting Presets Test

58-10 Adjusting Presets 7
Packet 0: STATE_FIND_DSPHASE0
Found EQ TS2 with tx_preset=7 and rx_preset=0 in packet 24804
Packet 24804: STATE_FIND_USPHASE0
Found Phase0 reflection of tx_preset=7 in upstream packet 24897
Packet 24897: STATE_FIND_DSPHASE1
Found start of Phase1 with FS=24 and LF=7 in downstream packet 76881
Packet 76881: STATE_FIND_USPHASE1
Recorded FS=34 and LF=12 from DUT in upstream packet 77041
Packet 77041: STATE_FIND_USPHASE3
Found start of Phase3 in upstream packet 121731
Packet 121731: STATE_FIND_DSPHASE3
Found start of Phase3 in downstream packet 121753
Packet 121753: STATE_FIND_RESPONSE
Validating upstream packet 121926
FAILURE:
Condition not met: (preset(6) == tx_preset(7))
Packet 121926: STATE_DONE
Verification Script Complete



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Making Sure Coefficients Match FS and LF Values Advertised in Phase 1

In Phase 3, the PTC transmits TS1s with EC=11b, with the Use Preset bit (symbol 6, bit 7) and Transmitter Preset values (symbol 6, bits 6:3) from a Test Case (starting at Test Case 1). The PTC must transmit these TS1 for at least 1 µs. The PTC shall obtain new block alignment every time it receives the new coefficients. The PTC should wait at least 1 µs and then check that the received TS1 contains the expected preset values for the Test Case. When the Expected Pre-Cursor, Cursor and Post-Cursor values are “any valid”, the received TS1 matches if all of the following are true (using FS and LF values captured in Step 5):

a) Pre-Cursor <= Floor (FS/4) 35

b) Pre-Cursor +Cursor +Post-Cursor = FS

c) Cursor – Pre-Cursor – Post-Cursor >= LF

If this check fails and the requested preset is not Reserved (e.g. 0x0 to 0xA), the DUT fails the test. If this check fails and the requested preset is Reserved (e.g. 0x0B to 0xF), the DUT is issued a warning.

In our example:

TEST CASE 7: Transmitter Preset = 0x6, Use Preset = 1,
Pre-Cursor = 0x01, Cursor = FS, Post-Cursor = 0x01

Expected Transmitter Preset = 0x6

Expected Reject Coefficient Values = 0

Expected Pre-Cursor, Cursor, and Post-Cursor = any valid

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Host Requests Preset 6
Device Accepts After 1.9 usec

Packet				Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols
121751	R←	8.0 x1	TS1	0	0	15	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 7 1	3	24	7	4A ...
121752	R←	8.0 x1	TS1	0	0	15	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 7 1	3	24	7	4A ...
121753	R→	8.0 x1	TS1	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 6 1	1	34	1	4A ...
121754	R←	8.0 x1	TS1	0	0	15	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 7 1	3	24	7	4A ...
121755	R→	8.0 x1	TS1	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 6 1	1	34	1	4A ...

- Test samples after 1.2 usec

Packet				Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols
121922	R←	8.0 x1	TS1	0	0	15	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 7 1	3	24	7	4A ...
121923	R→	8.0 x1	TS1	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 6 1	1	34	1	4A ...

- Device follows after 1.9 usec.

Packet				Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols
121950	R←	8.0 x1	TS1	0	0	15	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 6 1	4	30	0	4A ...

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Initial Preset Setting in Phase 0 Requested in Phase 3

Packets	Dir	Rate	Type	COM	Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	TS2 Symbols
17 TS Packets 29732-29763	R→	2.5 x1	TS2	K28.5	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, Autonomous Change, Speed Change	3 6	D05.2 ...

Packets	Dir	Rate	Type	Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	FS	LF	Post-Cursor	TS1 Symbols	Time Delta	Time St
97 TS Packets 76881-77097	R→	8.0 x1	TS1	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	1 0 7 0	24	7	5	4A ...	1.322 us	0001 . 906 0
33 TS Packets 77039-121729	R←	8.0 x1	TS1	0	0	15	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	1 0 6 0	34	12	0	4A ...	24.000 ms	0001 . 906 0

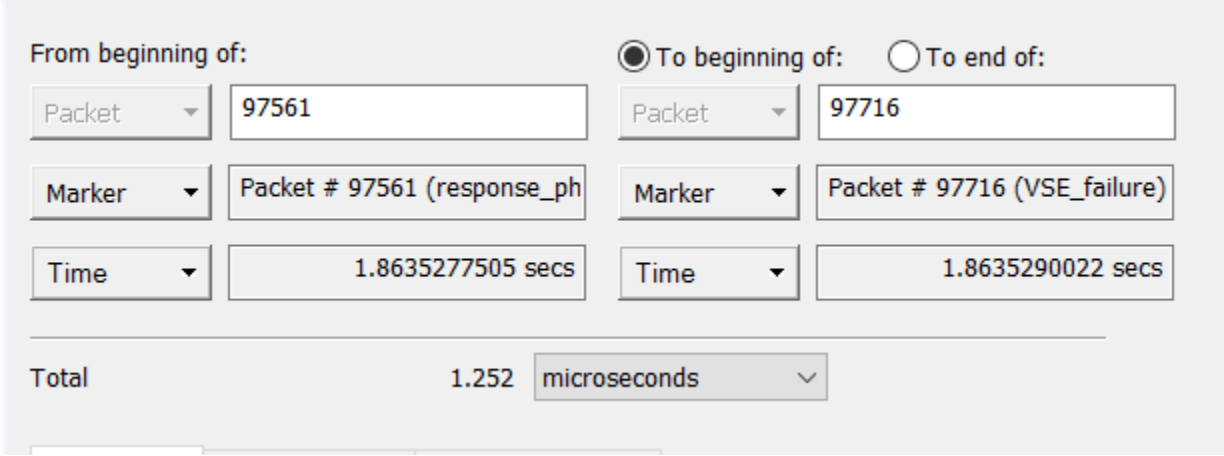
Packets	Dir	Rate	Type	Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor	TS1 Symbols	Time Delta
629 TS Packets 121730-123006	R←	8.0 x1	TS1	0	0	15	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 6 1	4	30	0	4A ...	366.750 ns
596 TS Packets 121753-122980	R→	8.0 x1	TS1	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 6 1	1	34	1	4A ...	10.000 us
38 TS Packets 122982-123060	R→	8.0 x1	TS1	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	0 0 7 0	2	17	5	4A ...	216.250 ns
17 TS Packets 123008-123039	R←	8.0 x1	TS1	0	0	15	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	0 0 6 0	4	30	0	4A ...	276.250 ns

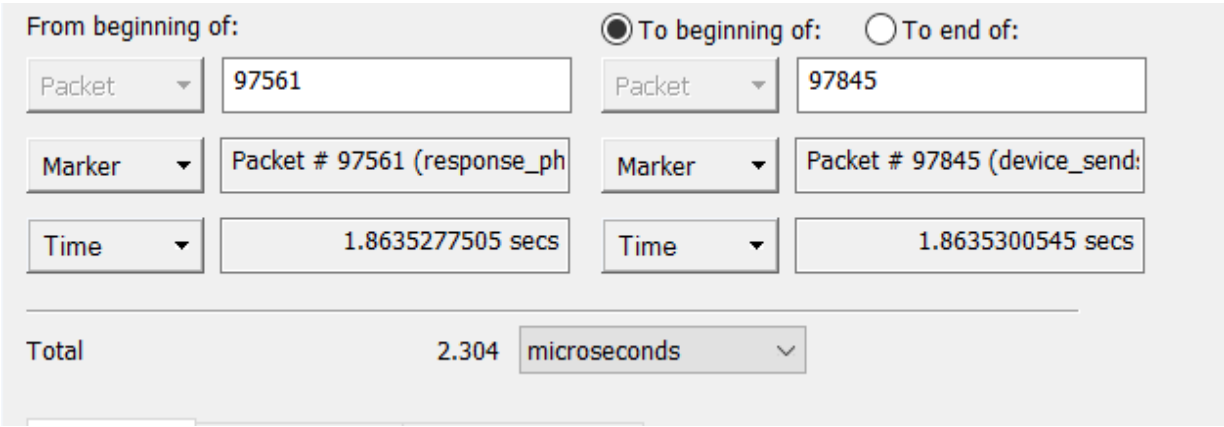
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Adjusting Coefficient Test

Time interval from initial request of coefficient to failure 1.2 usec

Time interval from initial request of coefficient to adjustment 2.3 usec





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Failure Log

Found start of Phase1 with FS=24 and LF=7 in downstream packet 52630
Packet#52630(2), Payload: 0x1E0000FF 0x0E003918 0x07854A4A
Packet 52630: STATE_FIND_USPHASE1
Packet#52849(1), Payload: 0x1E00000F 0x0E003922 0x0C874A4A
Recorded FS=34 and LF=12 from DUT in upstream packet 52851
Packet#52851(1), Payload: 0x1E00000F 0x0E003922 0x0C874A4A
Packet 52851: STATE_FIND_USPHASE3
Packet#97539(1), Payload: 0x1E00000F 0x0E00BB03 0x18874A4A
Found start of Phase3 in upstream packet 97540
Packet#97540(1), Payload: 0x1E00000F 0x0E00BB03 0x18874A4A
Packet 97540: STATE_FIND_DSPHASE3
Packet#97561(2), Payload: 0x1E0000FF 0x0E003B0B 0x00004A4A
Found response to requested coefficients in downstream packet 97561
Packet#97561(2), Payload: 0x1E0000FF 0x0E003B0B 0x00004A4A
Packet 97561: STATE_FIND_RESPONSE
Validating upstream packet 97716
Packet#97716(1), Payload: 0x1E00000F 0x0E00BB03 0x18874A4A
pre_cursor = 3, cursor = 24, post_cursor = 7, reject = 0
FAILURE: Unexpected response found in upstream packet 97716

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Coefficients Adjustment Process

Packet				Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor
97558	R←	8.0 x1	TS1	0	0	15	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 7 1	3	24	7
97559	R←	8.0 x1	TS1	0	0	15	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 7 1	3	24	7
97560	R←	8.0 x1	TS1	0	0	15	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 7 1	3	24	7
97561	R→	8.0 x1	TS1	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 7 0	11	0	0
97562	R←	8.0 x1	TS1	0	0	15	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 7 1	3	24	7
97563	R→	8.0 x1	TS1	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 7 0	11	0	0

Packet				Link	Lane	N_FTS	Training Control	Data Rate	Eq Control	Pre-Cursor	Cursor	Post-Cursor
97715	R→	8.0 x1	TS1	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 7 0	11	0	0
97716	R←	8.0 x1	TS1	0	0	15	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 7 1	3	24	7
97843	R←	8.0 x1	TS1	0	0	15	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 7 1	3	24	7
97844	R→	8.0 x1	TS1	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 7 0	11	0	0
97845	R←	8.0 x1	TS1	0	0	15	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 7 0	11	0	0
97846	R→	8.0 x1	TS1	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	3 0 7 0	11	0	0

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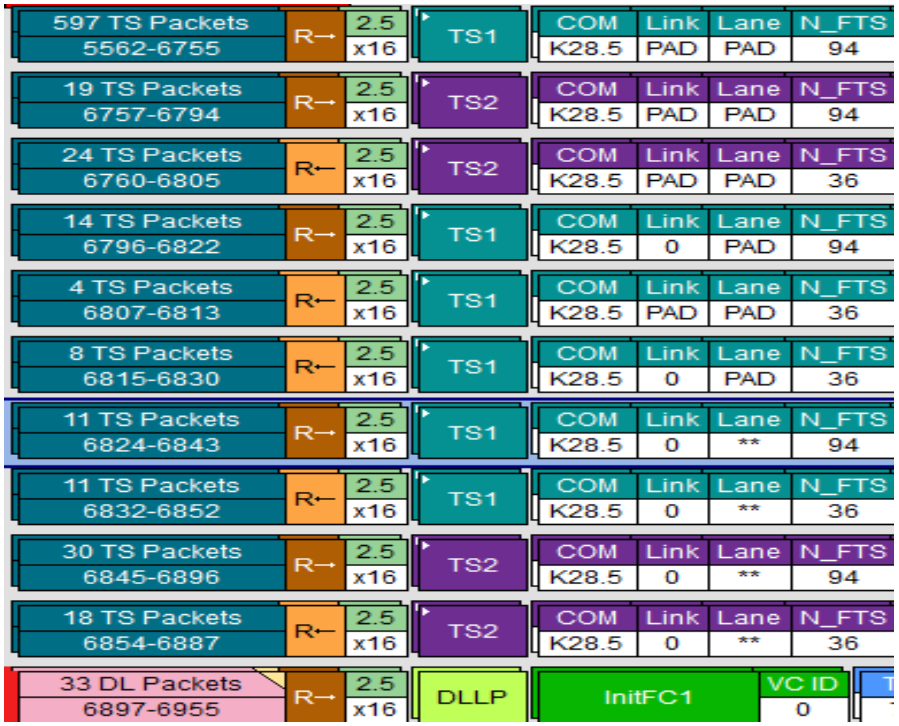
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Link/Lane Assignment Protocol

- Polling – TS1 / TS2 negotiation
- TS2 -> TS1 indicates transition to configuration
- Root assigns Link number
- EP follows
- Root assigns Lane numbers
- EP follows



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Test Case: Ruggedized Systems Technology Evolution

- Ruggedized blade server, VME, parallel PCI, PMC
- More bandwidth now required driven by more advanced sensors, radar systems etc.
- Platforms today focus on PCIe®
- Complex serial fabrics use point to point connections. Oftentimes they are assumed to work properly, but oftentimes there are interoperability issues that need to be addressed.

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Need a Tool to Debug the Link

Mobile all-weather air defense system designed to intercept and destroy short-range rockets and artillery shells fired from distances of 4 to 70 kilometers away and whose trajectory would take them to a populated area.



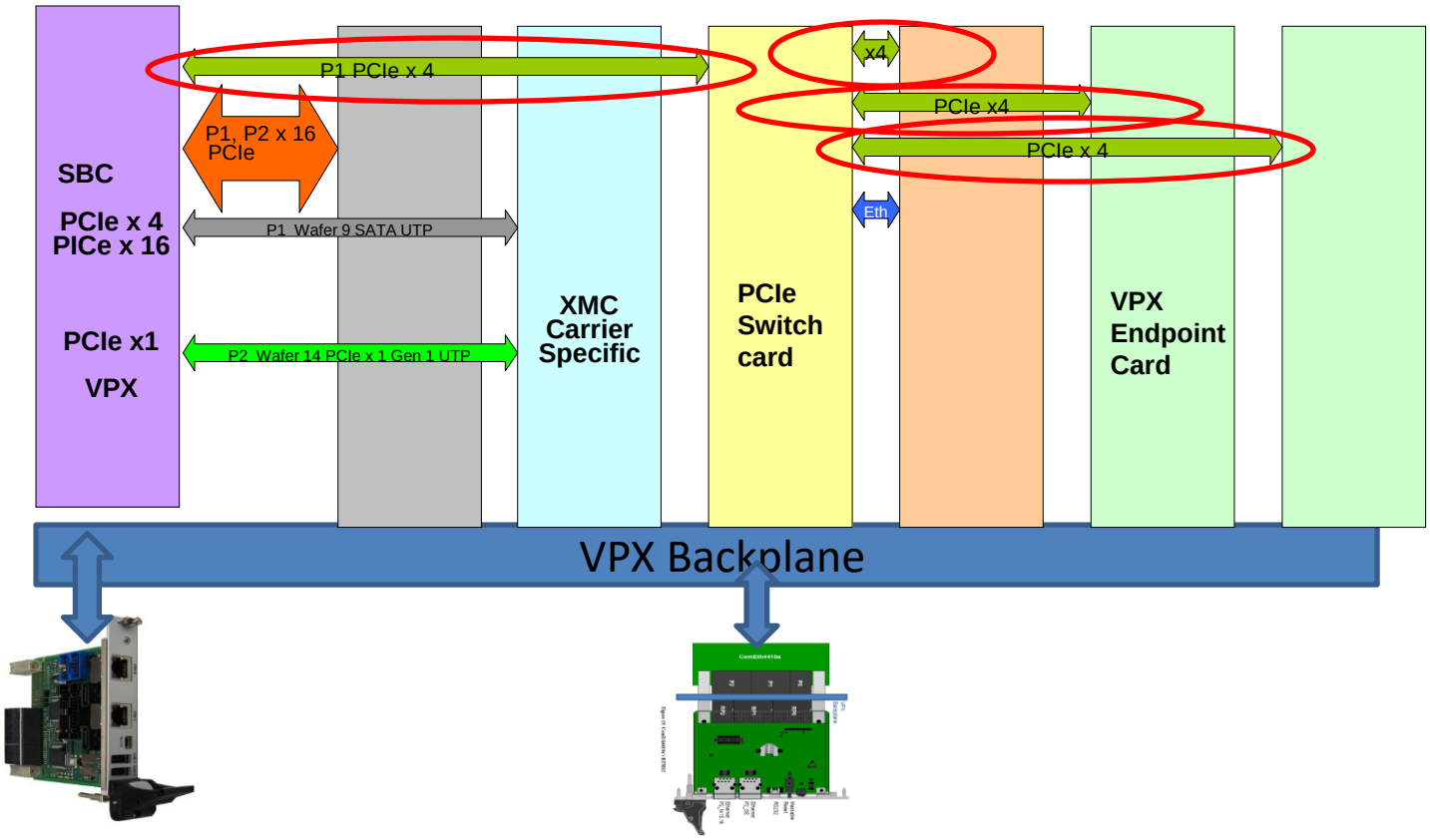
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Why a Tool to Debug the Serial Link?

- Things can go wrong in multiple places and throughput issues can occur in each of them.
- Trajectory analysis requires high performance
- Performance goals not met as anticipated by design
- Incorrect root cause analysis for low performance can result in delays in project completion
- Delay in deployment of launcher can cost lives

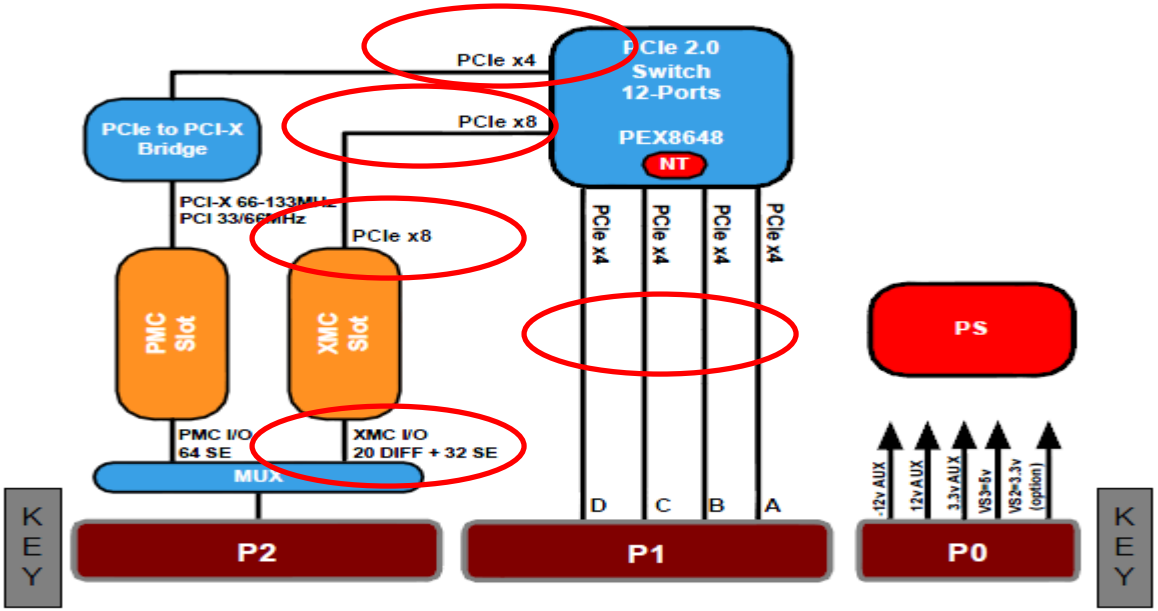
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Typical VPX Platform



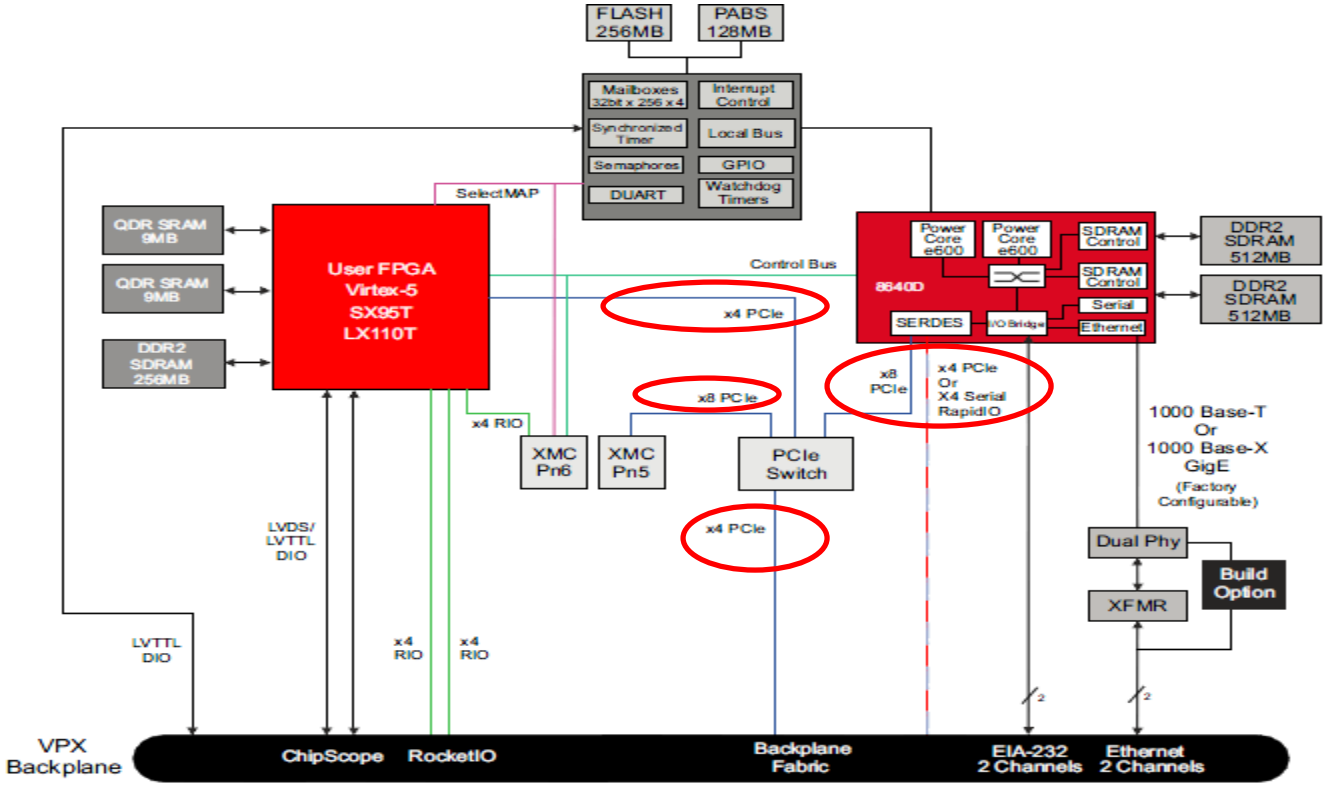
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VPX Switch Card Architecture



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VPX Endpoint Card Architecture



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VPX 3U Customer Problem Example

Problem: Our 3U VPX Endpoint works in all slots except for one slot.
We've been working for over a month to resolve this issue with our vendors to no avail.
We Suspect that we have an electrical/wiring/layout issue or backplane mismatch on that slot. We've completed extensive electrical tests and have been through a full schematic/layout review. All electrical and backplane issues have been eliminated as possible error sources but we think we may have to redo the layout.

Solution: Engage PCI Express Analyzer and VPX interposer to gain visibility into how the protocol was functioning to determine why the link would not train (failed to connect and be recognized by O/S in one slot on the backplane / worked fine in other slots).

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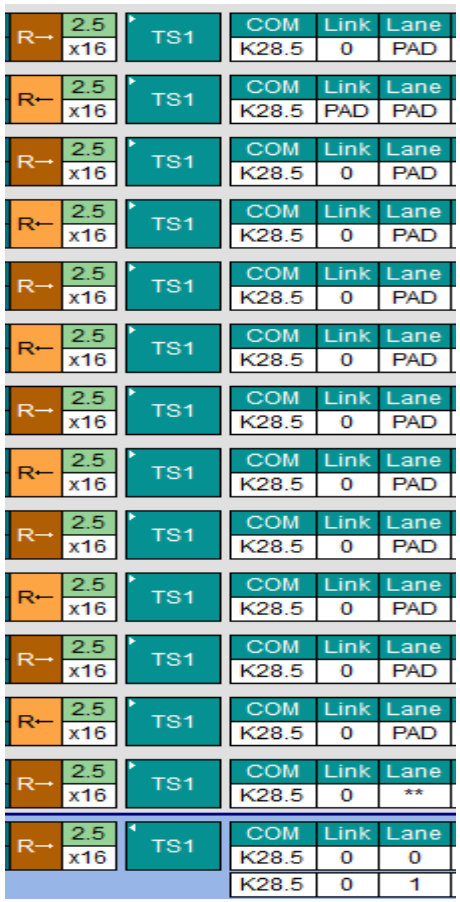
VPX 3U Problem Example

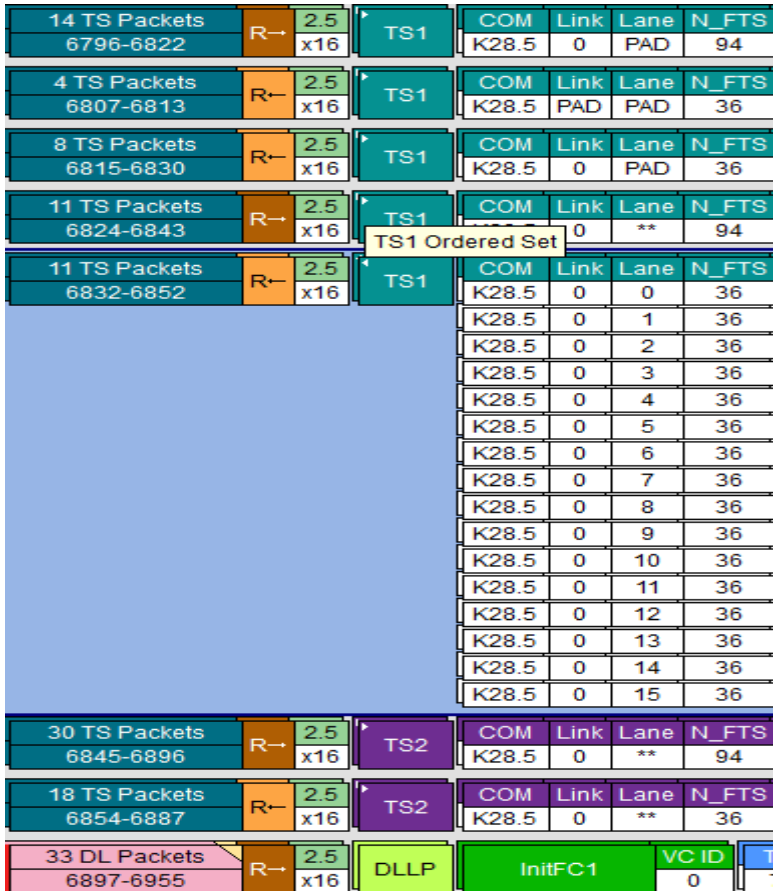
- First it has been determined that there is no electrical/layout issue since we got good clean captures with no errors.
- Second we put our attention to the trace and found protocol violations even in the good slot
- We then examine and identify the root cause for the failure as a protocol issue rather than an electrical or signal quality issue
- Customer can now go back to the vendor of the component exhibiting the protocol violation and provide evidence in a form of a trace exhibiting the failure
- Board vendor offered an upgrade solution that eliminated the problem
- We captured a trace with the upgraded board and found it still exhibits the protocol violation that just happens not to disrupt this particular platform but can cause a problem down the road on other platforms

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Compliant Link and Lane Assignments

- Configuration state link and lane assignments
- Root assigns link and lane numbers and EP follows
- Transition to L0

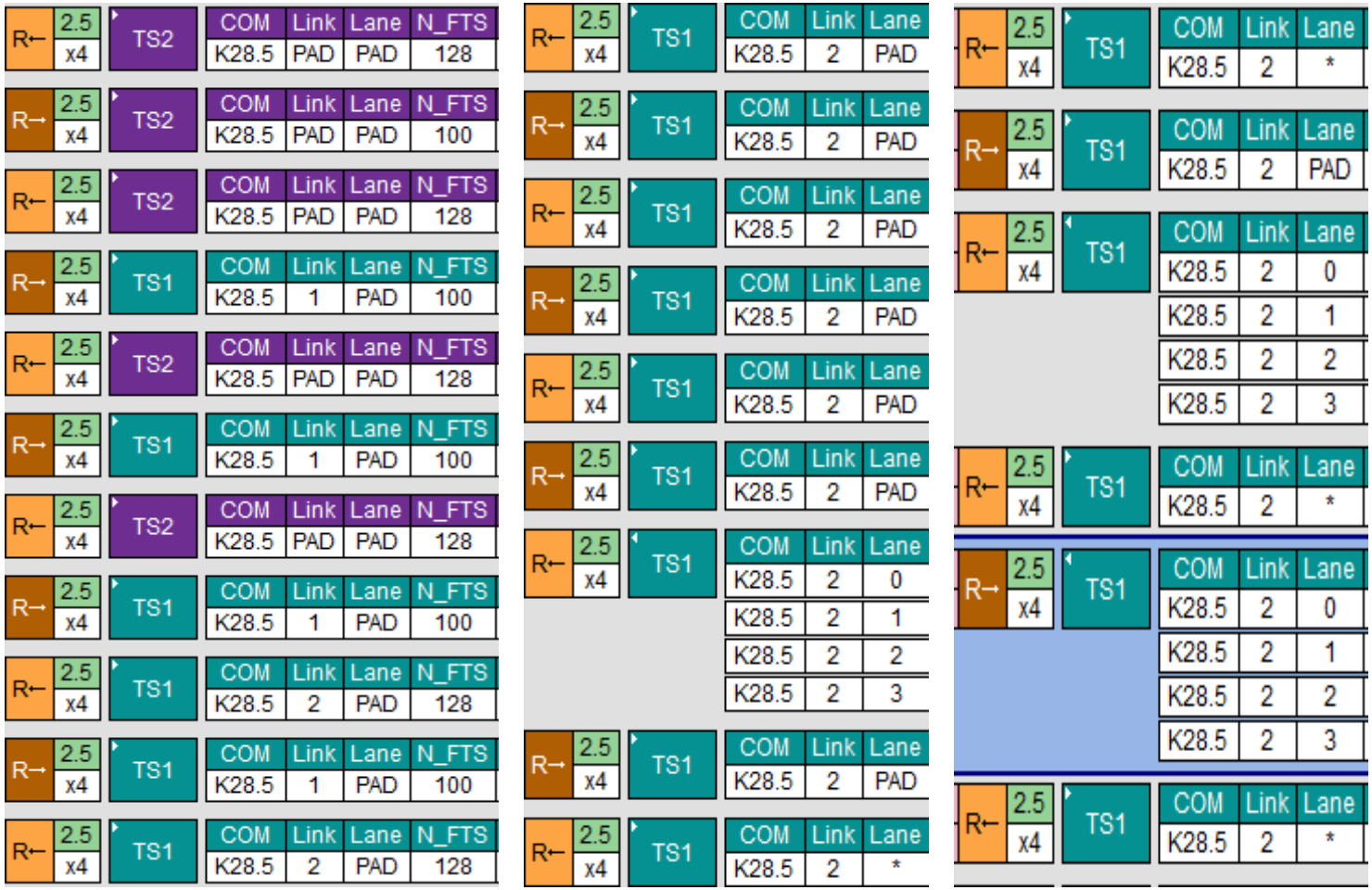




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EP Card in Slot 5, Incompliant Link Assignment

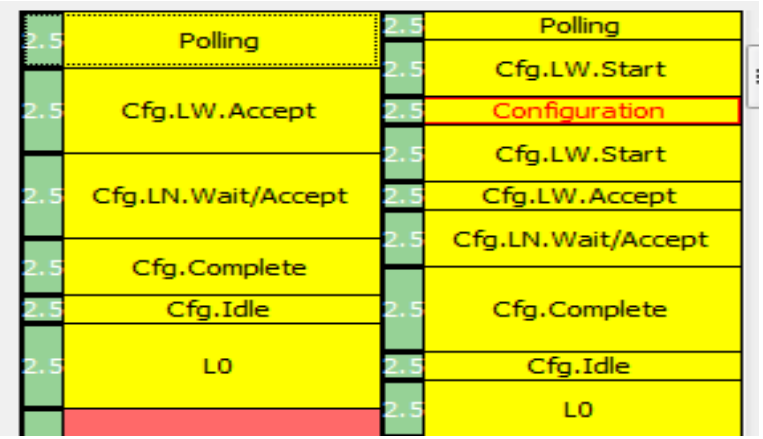
- Downstream port assigns link number 1
- Upstream port does not follow and assigns link number 2
- Upstream port assumes root role and assigns lane numbers
- Tool indicating protocol violation in configuration state

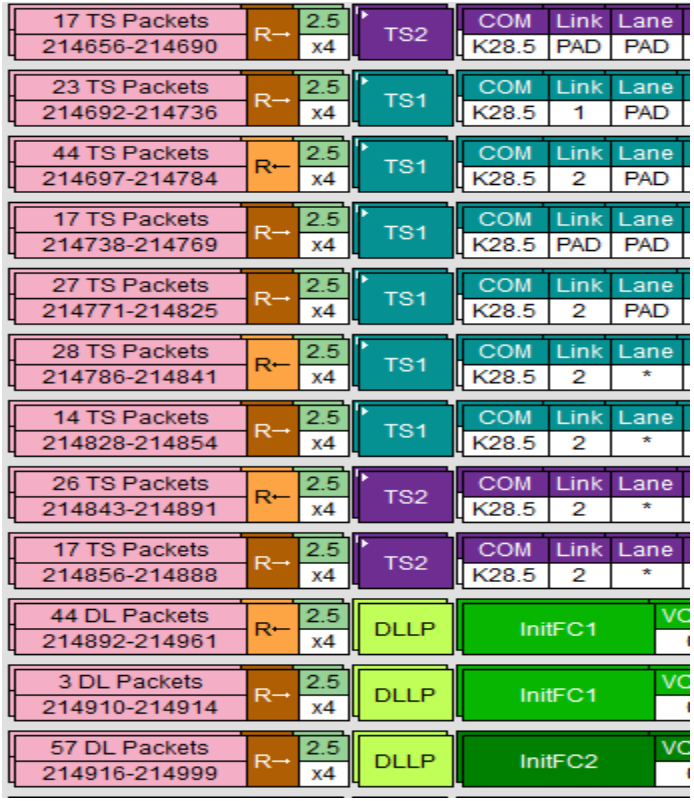


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EP Card in Slot 5, Compacted Trace

- Downstream port assigns link number 1
- Upstream port does not follow and assigns link number 2
- Upstream port assumes root role and assigns lane numbers
- Tool indicating protocol violation in configuration state

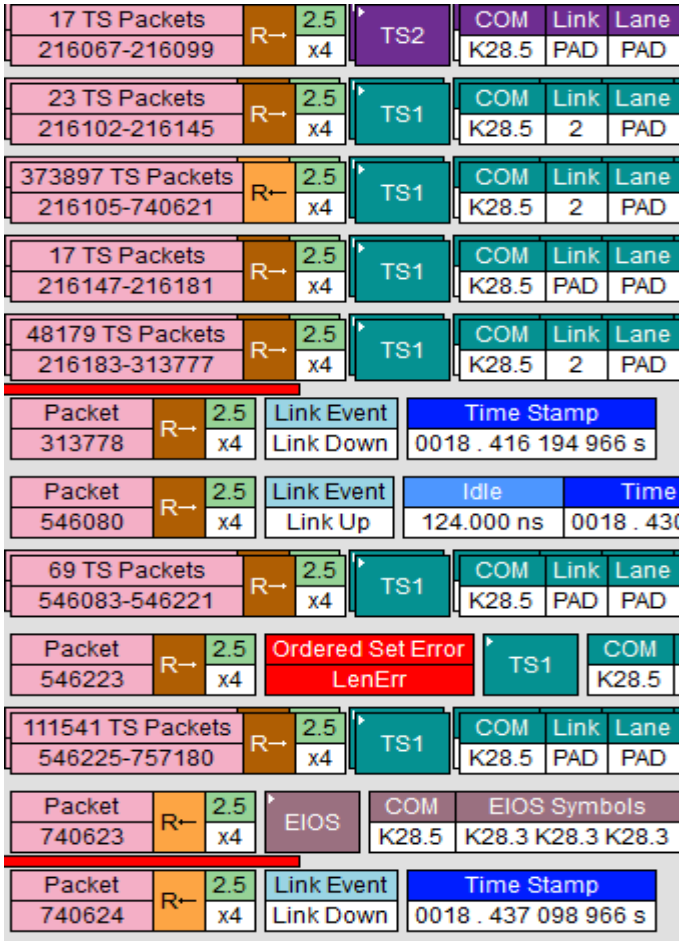




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EP Card in Slot 6, Compacted Trace

- Downstream port assigns link number 2
- Upstream port assigns link number 2
- Upstream port assumes endpoint role since downstream port does not change link assignment to follow and fails to assign lane numbers
- Downstream port assumes endpoint role as well since upstream port does not change link assignment to follow and fails to assign lane numbers
- Lane numbers are never assigned resulting in the link going down



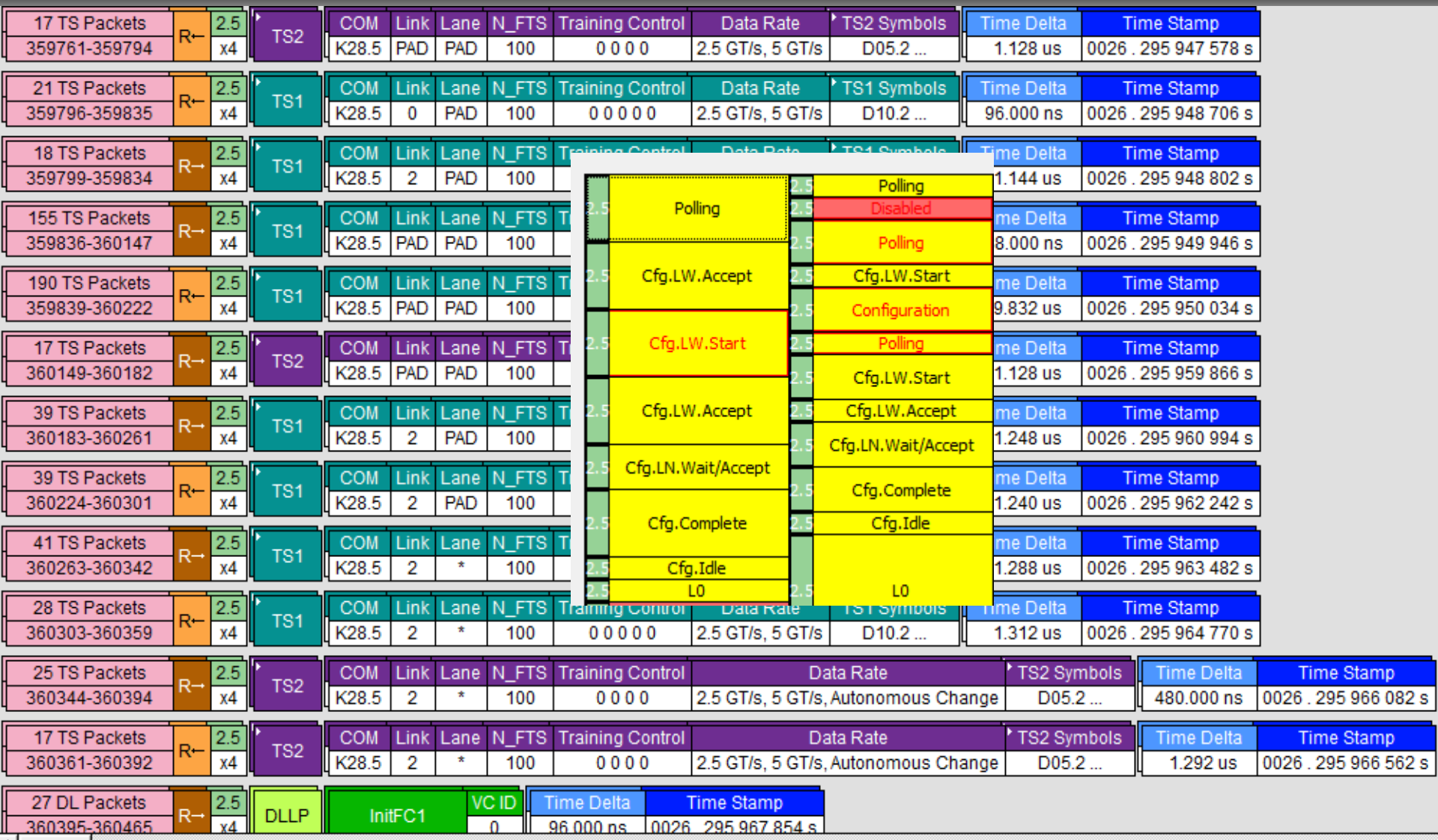
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Customer Solution

- "Ok then, we just won't use that particular Endpoint Card that isn't working"
  - Obtained a different vendor's Endpoint card and it worked fine in the previously non-working slot (a possible advancement on this issue)
  - Upon further testing, the New Endpoint does not work in other slots
  - The problem continues…..

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Upgraded Board Uses Link# 0



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Compliant Cross-Link Behavior

- A cross link consists of two link partners acting as downstream Ports.
- Downstream Lanes that detected a Receiver during Detect must first transmit 16-32 TS1 Ordered Sets with a non PAD Link number and PAD Lane number. Then any downstream Lanes that receive two consecutive TS1 Ordered Sets with a Link number different than PAD (K23.7) and a Lane Number set to PAD, are designated as Upstream Lanes and a random cross Link timeout is chosen
- When both Ports become Upstream the one with the shorter timeout becomes a Downstream Port and the other side remains an Upstream Port.
- The cross link timeout must be random even when hooking up two of the same devices so as to eventually break any possible deadlock.

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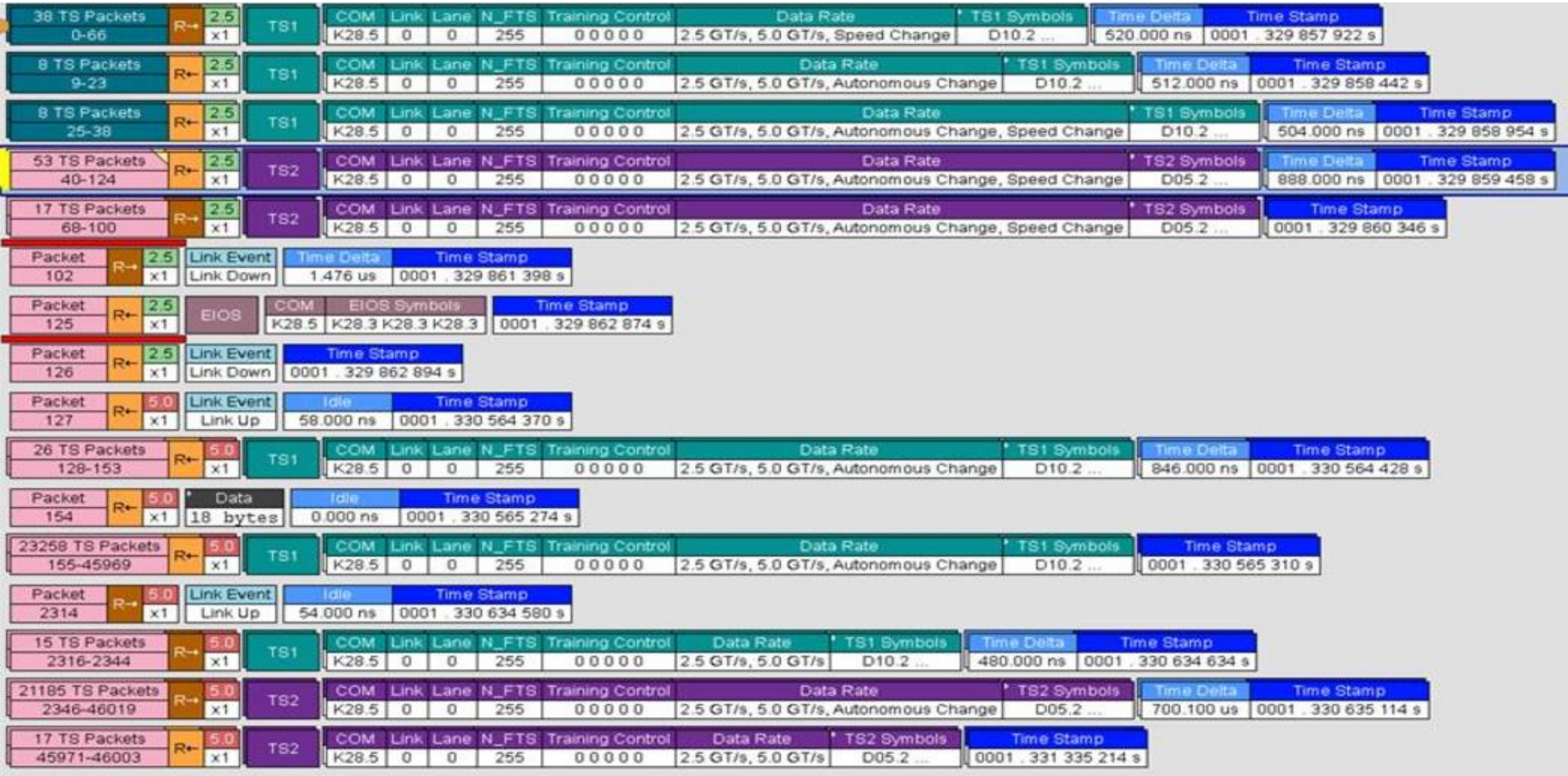
Ultimate Resolution

- Captures & analysis were completed on site with the customer in about 2 hours
- Determined that when both the Switch and Endpoint assign the same link number, the custom non-transparent bridging logic has a flaw.
- Datasheets for the Endpoint and Switch were consulted for clues to configuration issues
  - Non-Transparent bridging was enabled on the PCIe Switch (correctly)
  - System Implementation mode was not implemented on the Endpoint (Dual Root/Endpoint)
  - Both the Switch and Endpoint were trying to act as downstream ports
- Changed the Endpoint to “System Mode” (to act as an Endpoint)
- There was a bug in the Switch Vendor’s Custom Logic that needs correction
  - The Teledyne LeCroy Customer and Switch Vendor are now armed with sufficient information to work toward an ultimate engineering resolution

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Speed Transition with Incorrect TS2 Count

Link training TS2 packets in Rec.RcvrCfg are less than 32 TS2 as required



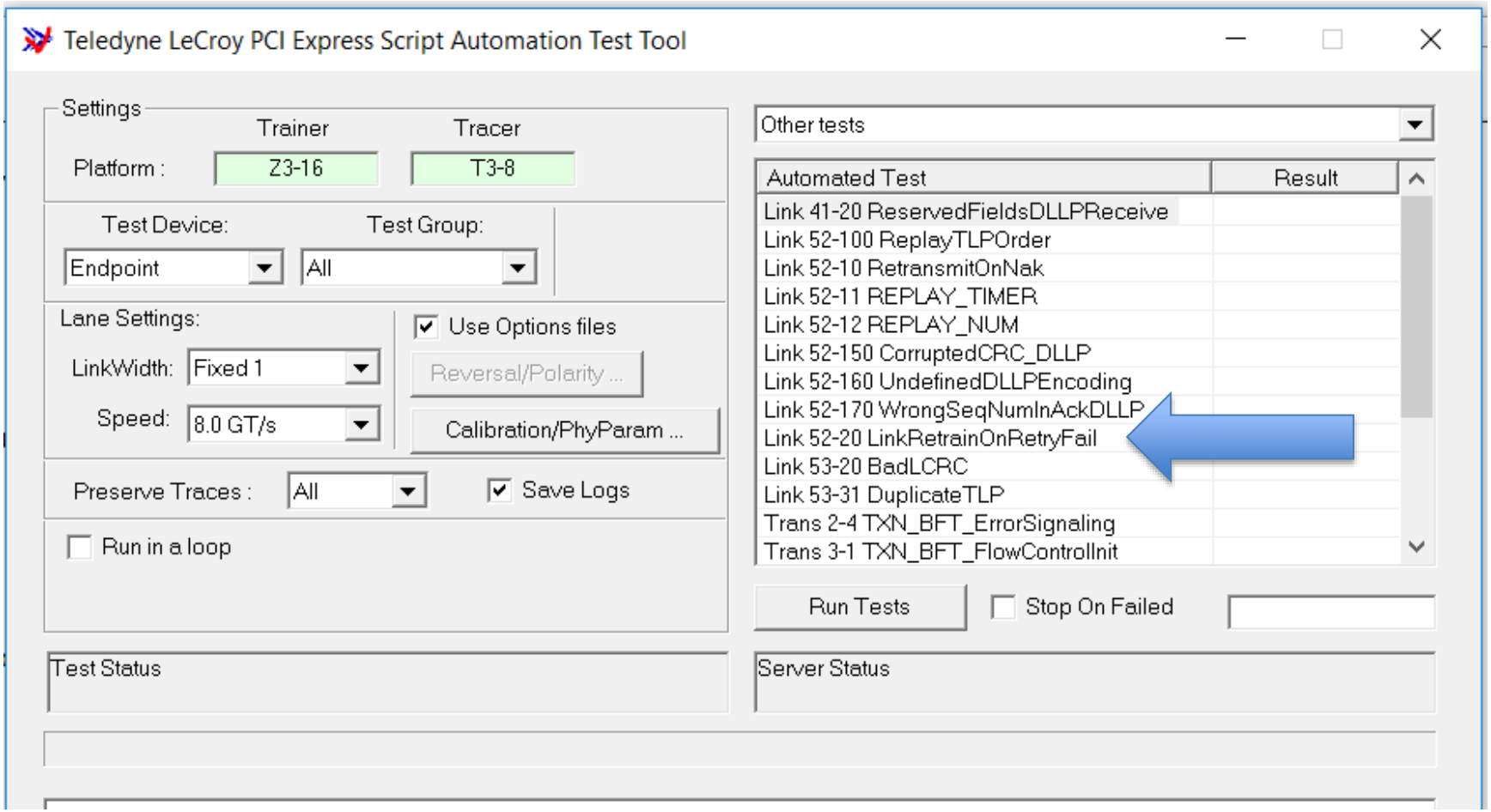
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Test Automation Tool



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Automation Script

```
TestAnalyzer =  PETracer   ;
TestGroup    = "Link Layer";

TestName     = "Link 52-20 LinkRetrainOnRetryFail";
TestCode     = "Test 52-20";

TestDescription = "The intent of this test is to ensure that the link connected to the DUT
will go into retraining after trying for REPLAY_NUM of times to get a TLP
through and failing. It will also test that while in retraining
the retry buffer and link states are not changed and the pending TLP
is retransmitted after link retraining completes.";

//AssertionsTested=DLL.5.2#2, DLL.5.2#7

RecordingOptions   = "Endpoint\\link_layer.rec";
GenerationOptions  = "Endpoint\\link_layer.gen";
TrainerScript      = "Endpoint\\LinkLayer\\link_52-20_LinkRetrainOnRetryFail.peg";

VerificationScript = "Endpoint\\LinkLayer\\link_52-20_LinkRetrainOnRetryFail.pevs";
GenerationTimeout = 3000;
```


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Generation Script

```
*  link_52-20_LinkRetrainOnRetryFail.peg                                    *
*  Trainer script for PCI Express Compliance Testing                          *
*    Brief Description: Link Layer Test 52-20 - LinkRetrainOnRetryFail.       *
*                  The intent of this test is to ensure that the link connected to the DUT    *
*                  will go into retraining after trying for REPLAY_NUM of times to get a TLP  *
*                  through and failing.

/* Switch to the 'No Ack or Nak' ACK/NAK policy */
Config=AckNak {    AckNak = Disable ; Nak}
/* Request a configuration read of register 0 (Device and Vendor IDs) */
packet="Temp_ConfigRead0"{    Tag = VAR_CURRENT_SEQUENCE_NUMBER_XMT}
/* Allow the REPLAY timer to expire for REPLAY_NUM + 1 times to cause link retrain */
wait=LinkCondition{    Conditions = TS1    Timeout = 4000000}
/* Switch back to the 'Automatic' ACK/NAK policy */
Config=AckNak{    AckNak = Ack}
/* Wait for the replayed Configuration Read Completion (with data)        */
/* The DUT is supposed to retrain  the link and resend the Completion TLP */
wait=TLP{       TLPType = CplD}
wait = 5000;
wait=DLLP{    DLLPType = UpdateFc_P}
/* Switch back to the 'Automatic' ACK/NAK policy */
Config=AckNak{    AckNak = Auto}
```


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VSE – Level, Channel and Type Settings

```
OnStartScript()
{
    ReportText( "Testing Link Layer 52-20 - LinkRetrainOnRetryFail.\n" );

    SendAllChannels();

    # to make sure that Split level is decoded before the script is called
    SendLevel( _PACKET );
    SendLevel( _SPLIT );

    SendTlpType       ( _PE_ALL_TYPES );
    SendDllpType      ( _PE_ALL_TYPES );
    SendOrderedSetType( _PE_ALL_TYPES );

    FilterDllpType( _DLLP_TYPE_INIT_FC );
    FilterDllpType( _DLLP_TYPE_UPDATE_FC );

    FilterOrderedSetType( _ORDSET_TYPE_FTS      );
    FilterOrderedSetType( _ORDSET_TYPE_IDLE_SET );
    FilterOrderedSetType( _ORDSET_TYPE_IDLE_GLC );
    FilterOrderedSetType( _ORDSET_TYPE_SKIP     );
    FilterOrderedSetType( _ORDSET_TYPE_PATN     );
}
```


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VSE – ProcessEvent

```
ProcessEvent()
{
   event_type = in.TraceEvent;

   select
   {
      event_type == _PKT_DLLP       : ProcessDllp();
      event_type == _PKT_TLP        :
      {
         # First TLP after Training Sequences signals the end of retraining
         if( InLinkRetraining )
         {
            # should observe TS1s and TS2s on both sides of the link for successful retraining
            if( NumTS1_DuringLinkRetrain[1] && NumTS1_DuringLinkRetrain[2] &&
               NumTS2_DuringLinkRetrain[1] && NumTS2_DuringLinkRetrain[2] )
            {
               ReportText( "\nSuccessful Link Retraining was observed." );

               LinkRetrainingObserved = 1;
            }

            InLinkRetraining = 0;
         }

         ProcessTlp();
      }

      event_type == _PKT_ORDERED_SET : ProcessOrderedSet();
   };

   return Complete();
}
```


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VSE – Test Stage Handler

```
# Function:    ProcessCfgReadRequest()
# Description: Processes Configuration Read Request TLPs.
# Used by:     ProcessTlp function.
ProcessCfgReadRequest()
{
   if( in.Channel != _CHANNEL_2 )
   {
      FailTest( "Configuration Read sent in Upstream direction" );
      return null;
   }

   # submit request to the configuration state machine
   if( !CfgRequestReceived( CFG_TYPE_READ ) )
   {
      return null;                # Failed sequence
   }

   select
   {
      TestStage == STAGE_CLEAR_ADV_CORRECTABLE_ERRS    : ProcessExpectedRead();
      TestStage == STAGE_MAIN_TEST                     : ProcessExpectedRead();
      TestStage == STAGE_READ_DEV_STATUS_REG           : ProcessExpectedRead();
      TestStage == STAGE_READ_ADV_UNCORRECTABLE_ERRS   : ProcessExpectedRead();

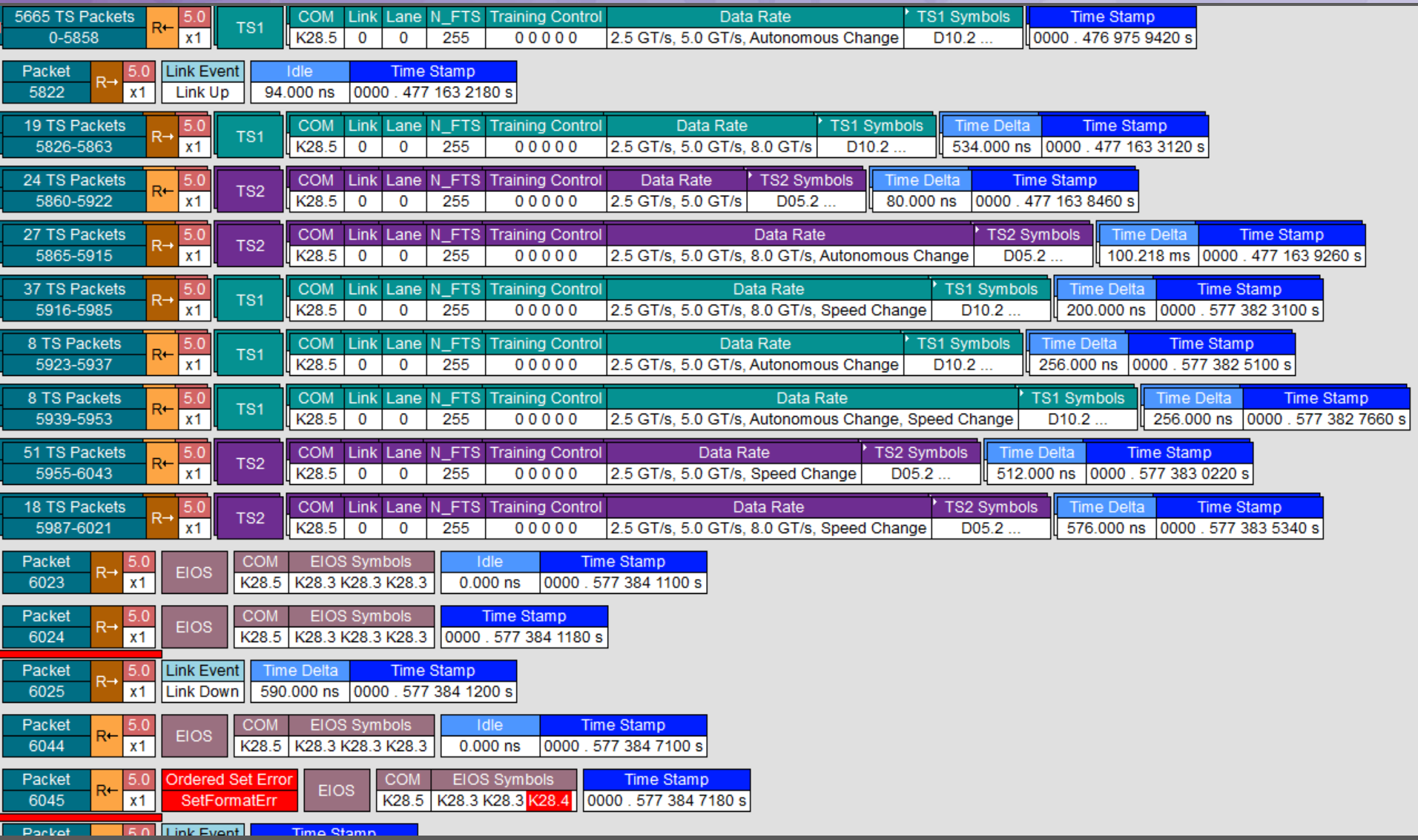
      TestStage == 0                                   : ProcessUnexpectedRead();
      TestStage == STAGE_ENABLE_ERROR_REPORTING        : ProcessUnexpectedRead();
      TestStage == STAGE_CLEAR_ADV_UNCORRECTABLE_ERRS  : ProcessUnexpectedRead();
      TestStage == STAGE_READ_ADV_CORRECTABLE_ERRS     : ProcessUnexpectedRead();
      TestStage == STAGE_DISABLE_ERROR_REPORTING       : ProcessUnexpectedRead();

      TestStage == STAGE_CLEAR_ADV_CORRECTABLE_ERRS2   : ProcessExpectedRead();
      TestStage == STAGE_MAIN_TEST2                    : ProcessExpectedRead();
      TestStage == STAGE_READ_DEV_STATUS_REG2          : ProcessExpectedRead();
      TestStage == STAGE_READ_ADV_UNCORRECTABLE_ERRS2  : ProcessExpectedRead();

      TestStage == STAGE_ENABLE_ERROR_REPORTING2       : ProcessUnexpectedRead();
      TestStage == STAGE_CLEAR_ADV_UNCORRECTABLE_ERRS2 : ProcessUnexpectedRead();
      TestStage == STAGE_READ_ADV_CORRECTABLE_ERRS2    : ProcessUnexpectedRead();
      TestStage == STAGE_DISABLE_ERROR_REPORTING2      : ProcessUnexpectedRead();
   };
}
```


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Link Retrain Test



5665 TS Packets 0-5858	R←	5.0 x1	TS1	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS1 Symbols	Time Stamp
				K28.5	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, Autonomous Change	D10.2 ...	0000 . 476 975 9420 s

Packet 5822	R→	5.0 x1	Link Event	Idle	Time Stamp
			Link Up	94.000 ns	0000 . 477 163 2180 s

19 TS Packets 5826-5863	R→	5.0 x1	TS1	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS1 Symbols	Time Delta	Time Stamp
				K28.5	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	D10.2 ...	534.000 ns	0000 . 477 163 3120 s

24 TS Packets 5860-5922	R←	5.0 x1	TS2	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS2 Symbols	Time Delta	Time Stamp
				K28.5	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s	D05.2 ...	80.000 ns	0000 . 477 163 8460 s

27 TS Packets 5865-5915	R→	5.0 x1	TS2	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS2 Symbols	Time Delta	Time Stamp
				K28.5	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, Autonomous Change	D05.2 ...	100.218 ms	0000 . 477 163 9260 s

37 TS Packets 5916-5985	R→	5.0 x1	TS1	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS1 Symbols	Time Delta	Time Stamp
				K28.5	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, Speed Change	D10.2 ...	200.000 ns	0000 . 577 382 3100 s

8 TS Packets 5923-5937	R←	5.0 x1	TS1	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS1 Symbols	Time Delta	Time Stamp
				K28.5	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, Autonomous Change	D10.2 ...	256.000 ns	0000 . 577 382 5100 s

8 TS Packets 5939-5953	R←	5.0 x1	TS1	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS1 Symbols	Time Delta	Time Stamp
				K28.5	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, Autonomous Change, Speed Change	D10.2 ...	256.000 ns	0000 . 577 382 7660 s

51 TS Packets 5955-6043	R←	5.0 x1	TS2	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS2 Symbols	Time Delta	Time Stamp
				K28.5	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, Speed Change	D05.2 ...	512.000 ns	0000 . 577 383 0220 s

18 TS Packets 5987-6021	R→	5.0 x1	TS2	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS2 Symbols	Time Delta	Time Stamp
				K28.5	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, Speed Change	D05.2 ...	576.000 ns	0000 . 577 383 5340 s

Packet 6023	R→	5.0 x1	EIOS	COM	EIOS Symbols	Idle	Time Stamp
				K28.5	K28.3 K28.3 K28.3	0.000 ns	0000 . 577 384 1100 s

Packet 6024	R→	5.0 x1	EIOS	COM	EIOS Symbols	Time Stamp
				K28.5	K28.3 K28.3 K28.3	0000 . 577 384 1180 s

Packet 6025	R→	5.0 x1	Link Event	Time Delta	Time Stamp
			Link Down	590.000 ns	0000 . 577 384 1200 s

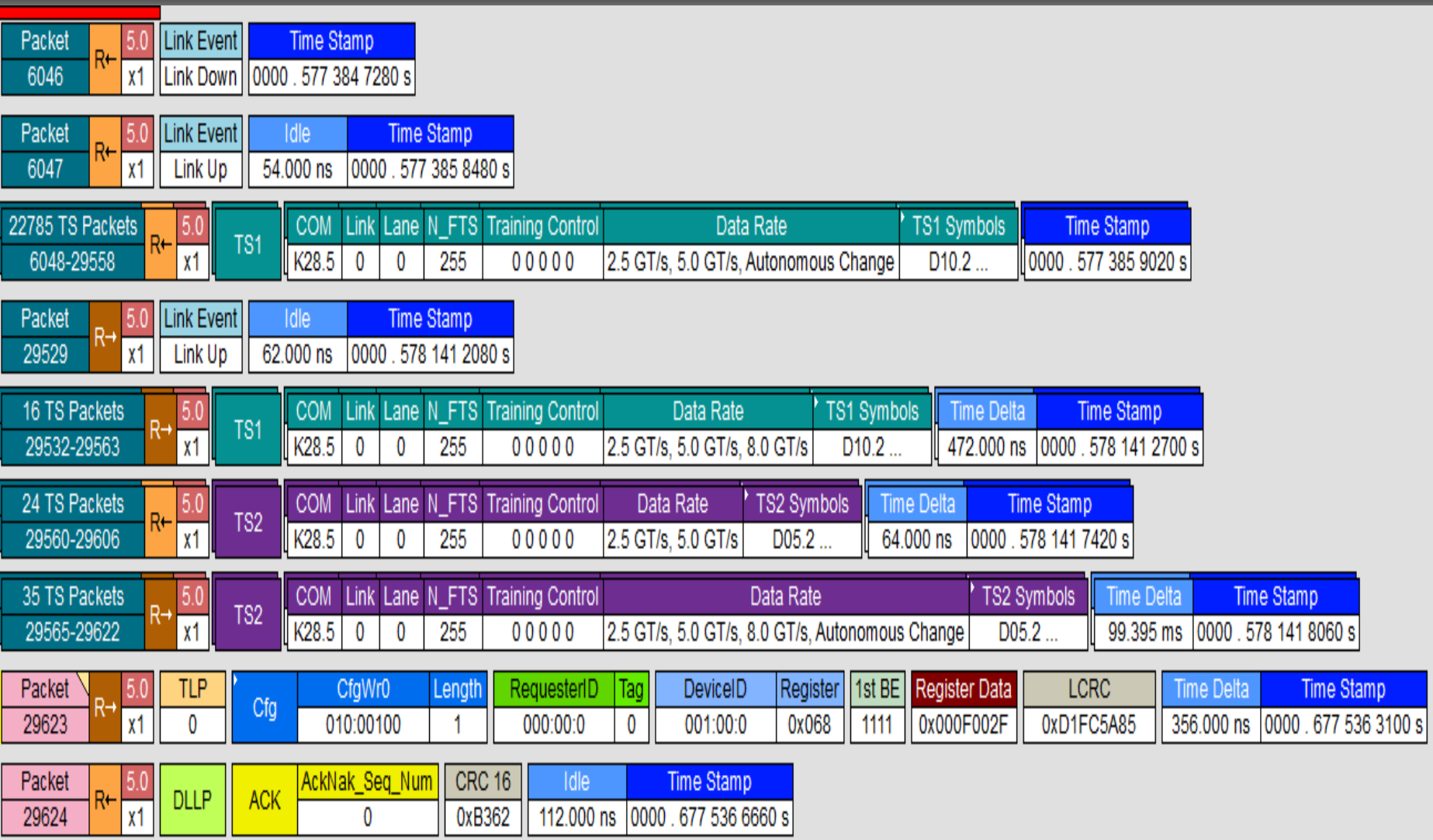
Packet 6044	R←	5.0 x1	EIOS	COM	EIOS Symbols	Idle	Time Stamp
				K28.5	K28.3 K28.3 K28.3	0.000 ns	0000 . 577 384 7100 s

Packet 6045	R←	5.0 x1	Ordered Set Error SetFormatErr	EIOS	COM	EIOS Symbols	Time Stamp
					K28.5	K28.3 K28.3 K28.4	0000 . 577 384 7180 s

Packet		5.0	Link Event	Time Stamp

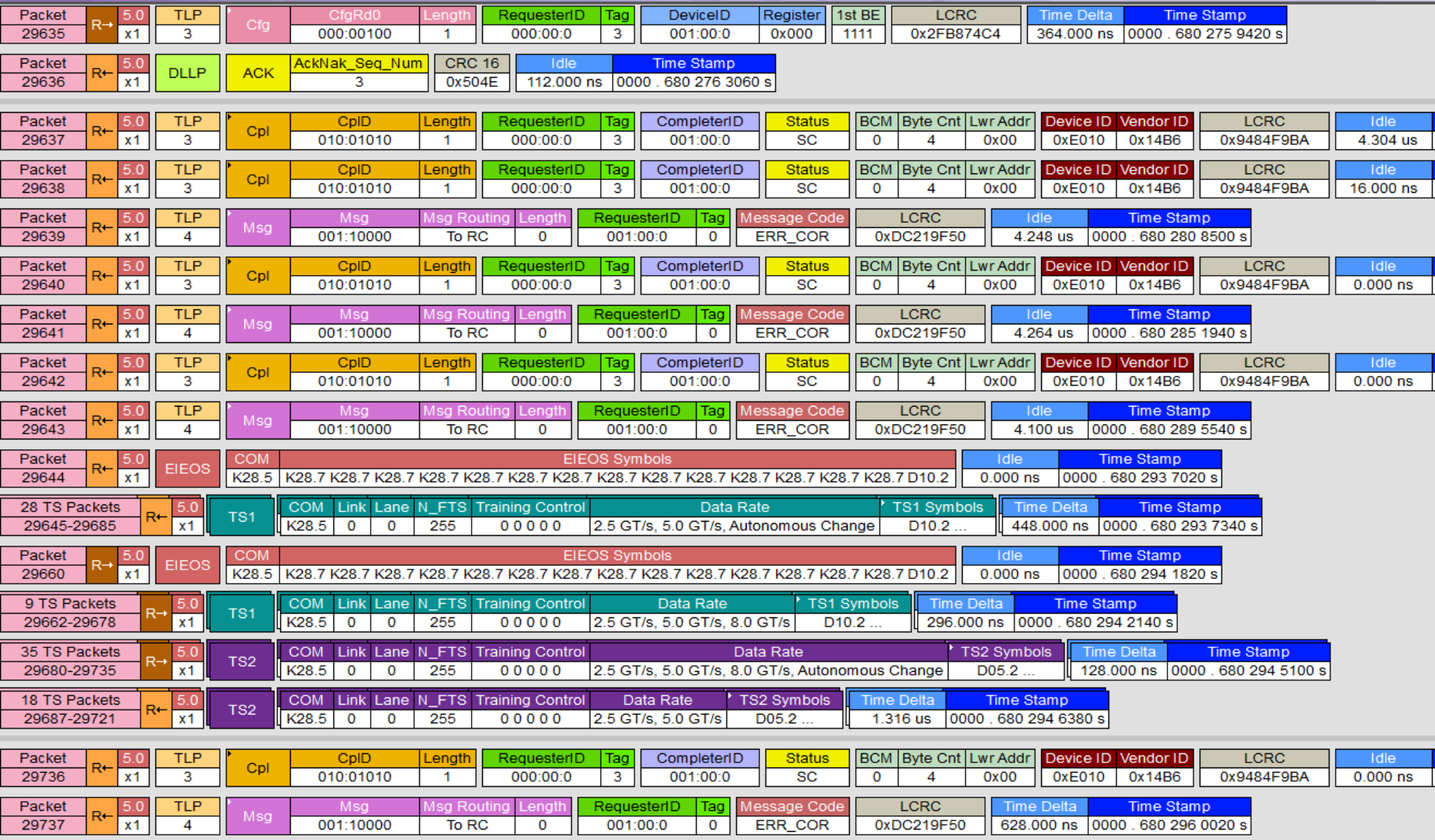
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Link Retrain Test



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Link Retrain Test



Packet			TLP		CfgRd0	Length	RequesterID	Tag	DeviceID	Register	1st BE	LCRC	Time Delta	Time Stamp
29635	R→	5.0 x1	3	Cfg	000:00100	1	000:00:0	3	001:00:0	0x000	1111	0x2FB874C4	364.000 ns	0000 . 680 275 9420 s

Packet			DLLP		AckNak_Seq_Num	CRC 16	Idle	Time Stamp
29636	R←	5.0 x1		ACK	3	0x504E	112.000 ns	0000 . 680 276 3060 s

Packet			TLP		CplD	Length	RequesterID	Tag	CompleterID	Status	BCM	Byte Cnt	Lwr Addr	Device ID	Vendor ID	LCRC	Idle
29637	R←	5.0 x1	3	Cpl	010:01010	1	000:00:0	3	001:00:0	SC	0	4	0x00	0xE010	0x14B6	0x9484F9BA	4.304 us
29638	R←	5.0 x1	3	Cpl	010:01010	1	000:00:0	3	001:00:0	SC	0	4	0x00	0xE010	0x14B6	0x9484F9BA	16.000 ns

Packet			TLP		Msg	Msg Routing	Length	RequesterID	Tag	Message Code	LCRC	Idle	Time Stamp
29639	R←	5.0 x1	4	Msg	001:10000	To RC	0	001:00:0	0	ERR_COR	0xDC219F50	4.248 us	0000 . 680 280 8500 s

Packet			TLP		CplD	Length	RequesterID	Tag	CompleterID	Status	BCM	Byte Cnt	Lwr Addr	Device ID	Vendor ID	LCRC	Idle
29640	R←	5.0 x1	3	Cpl	010:01010	1	000:00:0	3	001:00:0	SC	0	4	0x00	0xE010	0x14B6	0x9484F9BA	0.000 ns

Packet			TLP		Msg	Msg Routing	Length	RequesterID	Tag	Message Code	LCRC	Idle	Time Stamp
29641	R←	5.0 x1	4	Msg	001:10000	To RC	0	001:00:0	0	ERR_COR	0xDC219F50	4.264 us	0000 . 680 285 1940 s

Packet			TLP		CplD	Length	RequesterID	Tag	CompleterID	Status	BCM	Byte Cnt	Lwr Addr	Device ID	Vendor ID	LCRC	Idle
29642	R←	5.0 x1	3	Cpl	010:01010	1	000:00:0	3	001:00:0	SC	0	4	0x00	0xE010	0x14B6	0x9484F9BA	0.000 ns

Packet			TLP		Msg	Msg Routing	Length	RequesterID	Tag	Message Code	LCRC	Idle	Time Stamp
29643	R←	5.0 x1	4	Msg	001:10000	To RC	0	001:00:0	0	ERR_COR	0xDC219F50	4.100 us	0000 . 680 289 5540 s

Packet			EIEOS	COM	EIEOS Symbols	Idle	Time Stamp
29644	R←	5.0 x1		K28.5	K28.7 K28.7 K28.7 K28.7 K28.7 K28.7 K28.7 K28.7 K28.7 K28.7 K28.7 K28.7 K28.7 K28.7 D10.2	0.000 ns	0000 . 680 293 7020 s

28 TS Packets			TS1	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS1 Symbols	Time Delta	Time Stamp
29645-29685	R←	5.0 x1		K28.5	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, Autonomous Change	D10.2 ...	448.000 ns	0000 . 680 293 7340 s

Packet			EIEOS	COM	EIEOS Symbols	Idle	Time Stamp
29660	R→	5.0 x1		K28.5	K28.7 K28.7 K28.7 K28.7 K28.7 K28.7 K28.7 K28.7 K28.7 K28.7 K28.7 K28.7 K28.7 K28.7 D10.2	0.000 ns	0000 . 680 294 1820 s

9 TS Packets			TS1	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS1 Symbols	Time Delta	Time Stamp
29662-29678	R→	5.0 x1		K28.5	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s	D10.2 ...	296.000 ns	0000 . 680 294 2140 s

35 TS Packets			TS2	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS2 Symbols	Time Delta	Time Stamp
29680-29735	R→	5.0 x1		K28.5	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s, 8.0 GT/s, Autonomous Change	D05.2 ...	128.000 ns	0000 . 680 294 5100 s

18 TS Packets			TS2	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS2 Symbols	Time Delta	Time Stamp
29687-29721	R←	5.0 x1		K28.5	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s	D05.2 ...	1.316 us	0000 . 680 294 6380 s

Packet			TLP		CplD	Length	RequesterID	Tag	CompleterID	Status	BCM	Byte Cnt	Lwr Addr	Device ID	Vendor ID	LCRC	Idle
29736	R←	5.0 x1	3	Cpl	010:01010	1	000:00:0	3	001:00:0	SC	0	4	0x00	0xE010	0x14B6	0x9484F9BA	0.000 ns

Packet			TLP		Msg	Msg Routing	Length	RequesterID	Tag	Message Code	LCRC	Time Delta	Time Stamp
29737	R←	5.0 x1	4	Msg	001:10000	To RC	0	001:00:0	0	ERR_COR	0xDC219F50	628.000 ns	0000 . 680 296 0020 s

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Link Retrain Test

18 TS Packets	R←	5.0	TS2	COM	Link	Lane	N_FTS	Training Control	Data Rate	TS2 Symbols	Time Delta	Time Stamp
29687-29721		x1		K28.5	0	0	255	0 0 0 0 0	2.5 GT/s, 5.0 GT/s	D05.2 ...	1.316 us	0000 . 680 294 6380 s

Packet	R←	5.0	TLP	Cpl	CplD	Length	RequesterID	Tag	CompleterID	Status	BCM	Byte Cnt	Lwr Addr	Device ID	Vendor ID	LCRC
29736		x1	3		010:01010	1	000:00:0	3	001:00:0	SC	0	4	0x00	0xE010	0x14B6	0x9484F9

Packet	R←	5.0	TLP	Msg	Msg	Msg Routing	Length	RequesterID	Tag	Message Code	LCRC	Time Delta	Time Stamp
29737		x1	4		001:10000	To RC	0	001:00:0	0	ERR_COR	0xDC219F50	628.000 ns	0000 . 680 296 0020 s

Packet	R→	5.0	DLLP	ACK	AckNak_Seq_Num	CRC 16	Time Delta	Time Stamp
29738		x1			4	0x370C	452.000 ns	0000 . 680 296 6300 s

Packet	R←	5.0	TLP	Msg	Msg	Msg Routing	Length	RequesterID	Tag	Message Code	LCRC	Time Delta	Time Stamp
29739		x1	5		001:10000	To RC	0	001:00:0	0	ERR_COR	0x9FEA39D7	636.000 ns	0000 . 680 297 0820 s

Packet	R→	5.0	DLLP	ACK	AckNak_Seq_Num	CRC 16	Time Delta	Time Stamp
29740		x1			5	0x9617	460.000 ns	0000 . 680 297 7180 s

Packet	R←	5.0	TLP	Msg	Msg	Msg Routing	Length	RequesterID	Tag	Message Code	LCRC	Time Delta	Time Stamp
29741		x1	6		001:10000	To RC	0	001:00:0	0	ERR_COR	0x1BB1A384	636.000 ns	0000 . 680 298 1780 s

Packet	R→	5.0	DLLP	ACK	AckNak_Seq_Num	CRC 16	Time Delta	Time Stamp
29742		x1			6	0x753B	452.000 ns	0000 . 680 298 8140 s

Packet	R←	5.0	TLP	Msg	Msg	Msg Routing	Length	RequesterID	Tag	Message Code	LCRC	Time Delta	Time Stamp
29743		x1	7		001:10000	To RC	0	001:00:0	0	ERR_COR	0x587A0503	652.000 ns	0000 . 680 299 2660 s

Packet	R→	5.0	DLLP	ACK	AckNak_Seq_Num	CRC 16	Time Delta	Time Stamp
29744		x1			7	0xD420	460.000 ns	0000 . 680 299 9180 s

Packet	R←	5.0	TLP	Msg	Msg	Msg Routing	Length	RequesterID	Tag	Message Code	LCRC	Time Delta	Time Stamp
29745		x1	8		001:10000	To RC	0	001:00:0	0	ERR_COR	0x8D4987C5	652.000 ns	0000 . 680 300 3780 s

Packet	R→	5.0	DLLP	ACK	AckNak_Seq_Num	CRC 16	Idle	Time Stamp
29746		x1			8	0xBBBF	4.403 ms	0000 . 680 301 0300 s

Packet	R→	5.0	TLP	Cfg	CfgRd0	Length	RequesterID	Tag	DeviceID	Register	1st BE	LCRC	Time Delta	Time Stamp
29747		x1	4		000:00100	1	000:00:0	4	001:00:0	0x068	1100	0x751DCBA0	340.000 ns	0000 . 684 703 6300 s

Packet	R←	5.0	DLLP	ACK	AckNak_Seq_Num	CRC 16	Idle	Time Stamp
29748		x1			4	0x370C	112.000 ns	0000 . 684 703 9700 s

Packet	R←	5.0	TLP	Cpl	CplD	Length	RequesterID	Tag	CompleterID	Status	BCM	Byte Cnt	Lwr Addr	Register Data	LCRC
29749		x1	9		010:01010	1	000:00:0	4	001:00:0	SC	0	4	0x00	0x0001002F	0x9F0F64BD

Packet	R→	5.0	DLLP	ACK	AckNak_Seq_Num	CRC 16	Idle	Time Stamp
29750		x1			9	0x1AA4	1.234 ms	0000 . 684 704 6700 s

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Agenda

- Introduction
- Initial Training Analysis
- Transmitter and Receiver Equalization
- 8 Gig Speed Transition
- 16 Gig Speed Transition
- Violations Detected by PCI-SIG Compliance
- Violations Detected by Additional Validation Tests
- Automation of a Validation Test Suite
- **Summary**

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Summary

- Discussed analysis methods of link training and dynamic equalization
  - Cross link protocol example
- Showed traffic generation techniques for speed transition validation
  - Compliance and validation examples
- Failure examples covered by PCI-SIG Compliance
  - Example: Phase transition time limits
- Not all incompliant behaviors covered by PCI-SIG Compliance
  - Example: Link training TS2 packets in Rec.RcvrCfg are less than 32 TS2 as required
- Showed how to incorporate a sequence of validation tests into a test automation environment.

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